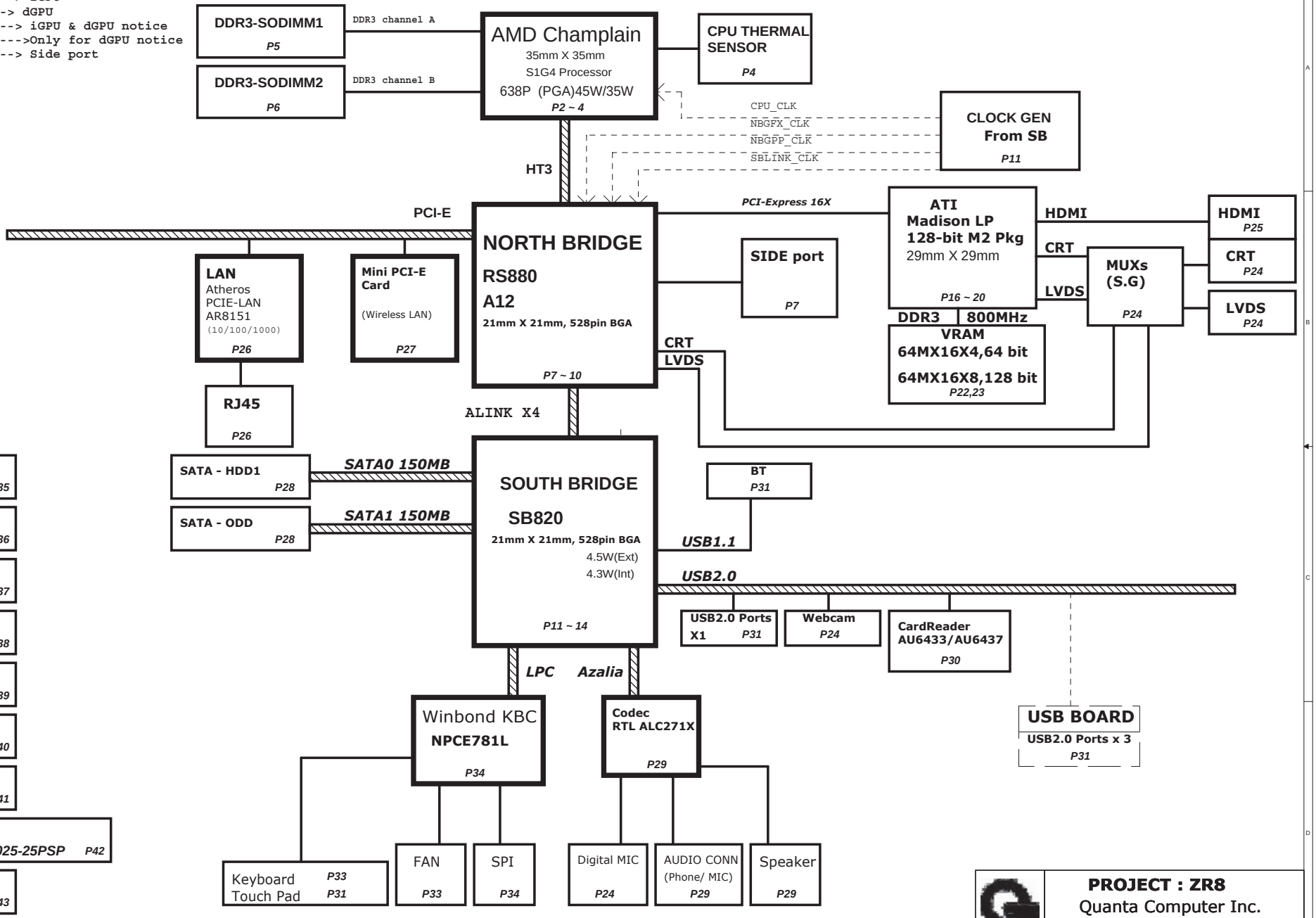
ZR8 SYSTEM DIAGRAM

RAMP

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

```
SGN@---->Internal CLK GEN.
GN@  ---->External CLK GEN.
IV@  -----> iGPU
SW@ -----> dGPU
SP@  -----> iGPU & dGPU notice
SPE@  ----->Only for dGPU notice
SIDE@ ----> Side port
```



Charger (ISL88731A) P35

DC/DC (3VPCU / 5VPCU)
RT8206B P36

CPU_VCORE (VCORE)
ISL6265A P37

DC/DC (+1.1V_S5)
UP6111AQD P38

DC/DC (NB_CORE)
UP6111AQD P39

DC/DC (+1.5VSUS)
RT8207A P40

DC/DC (GPU_CORE)
MAX8792ETD+T P41

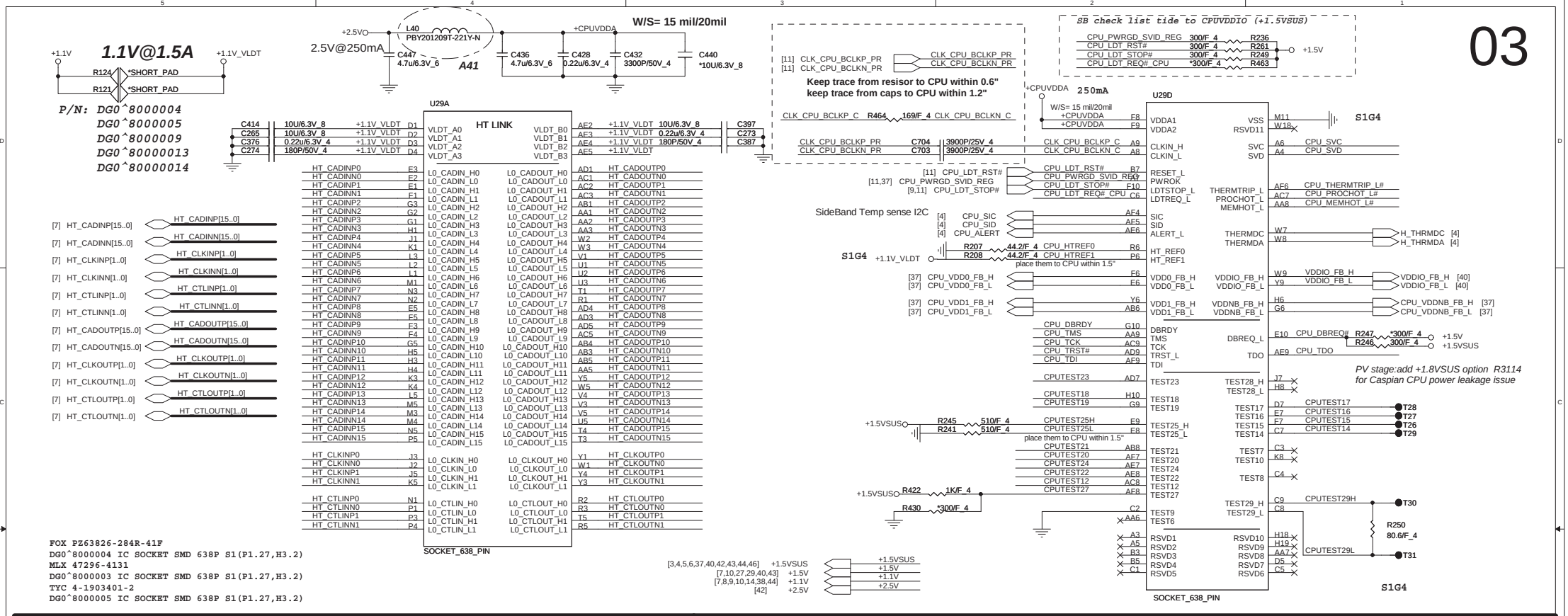
DC/DC (+1.8V/+1V/+2.5V)
HPA00835RTER / RT9018A / RT9025-25PSP P42

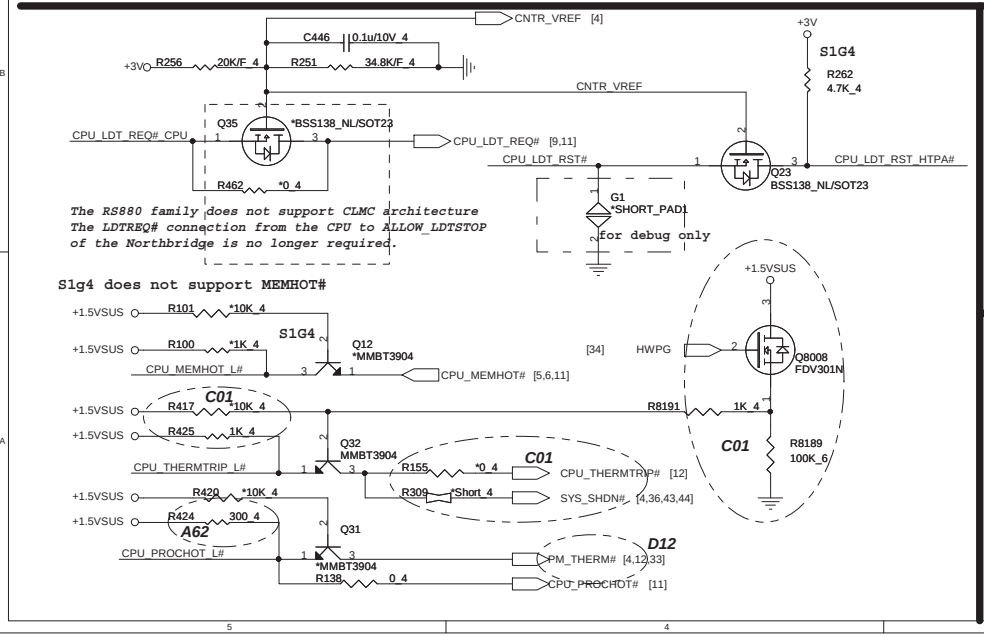
DC/DC (CPU_VDDR)
RT9025-25PSP P43

PROJECT : ZR8
Quanta Computer Inc.

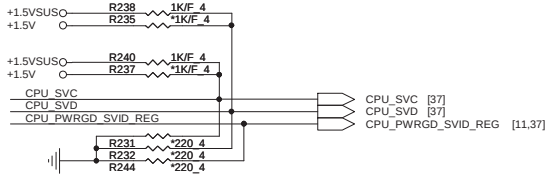
Size	Document Number	Rev
	Block Diagram	1A

Date: Wednesday, May 27, 2009 Sheet 1 of 49





Serial VID

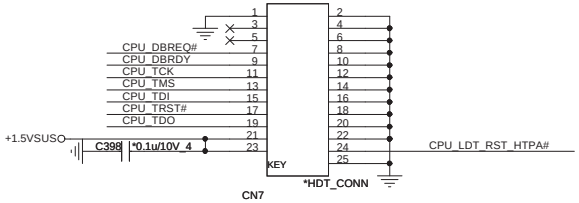


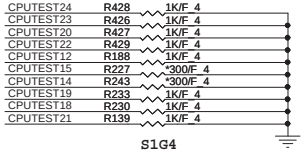
VFIX MODE — VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

S1G4

HDT Connector





S1G4

PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	S1G4 HT,CTL I/F 1/3	1A
Date: Wednesday, May 27, 2009	Sheet 2 of 49	

Processor Memory Interface

04

VDDR=>1.75A

VDDR=> 0.9V support 1066 / 800 DDR
VDDR= >1.05V support 1333 / 1066 / 800 DDR

PLACE THEM CLOSE TO CPU WITHIN 1"

U29B — MEM:CMD/CTRL/CLK

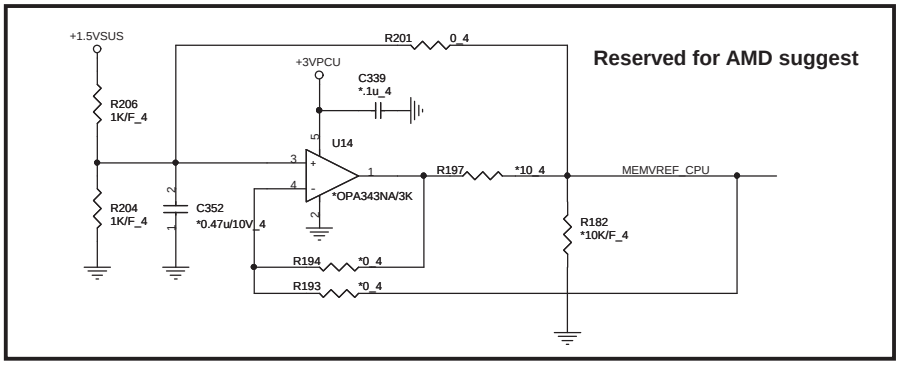
U29C — MEM:DATA

SOCKET_638_PIN

Place close to socket

Reserved for AMD suggest

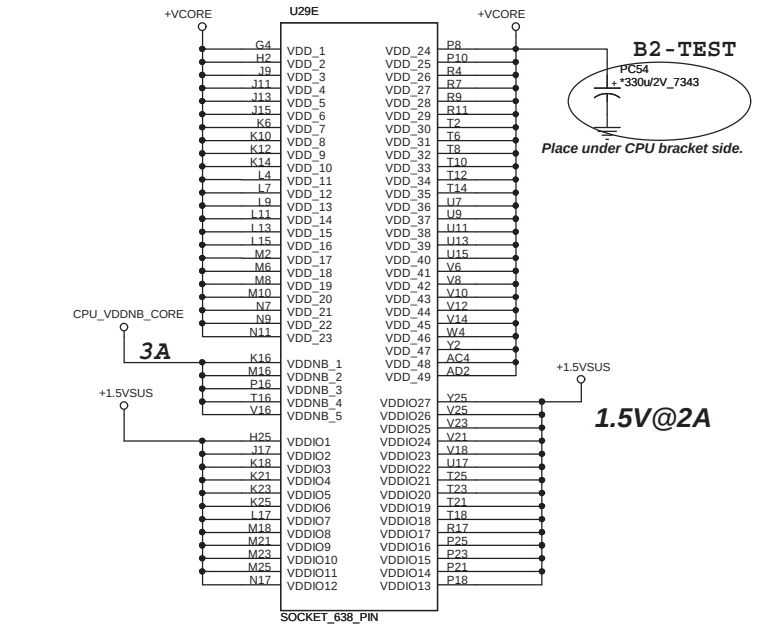
U14 *OPA343NA/3K

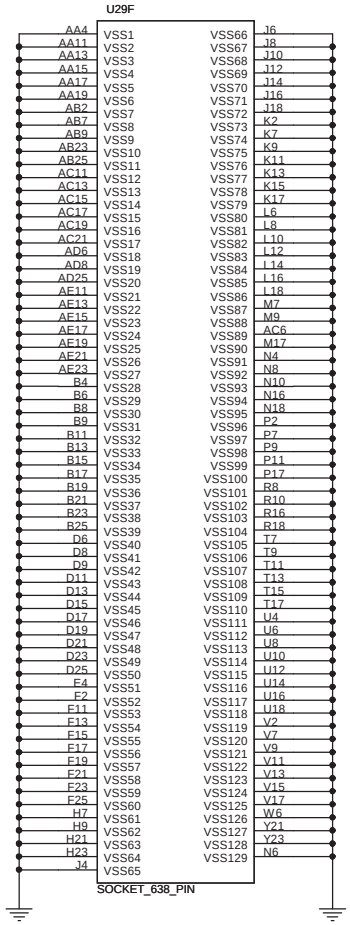


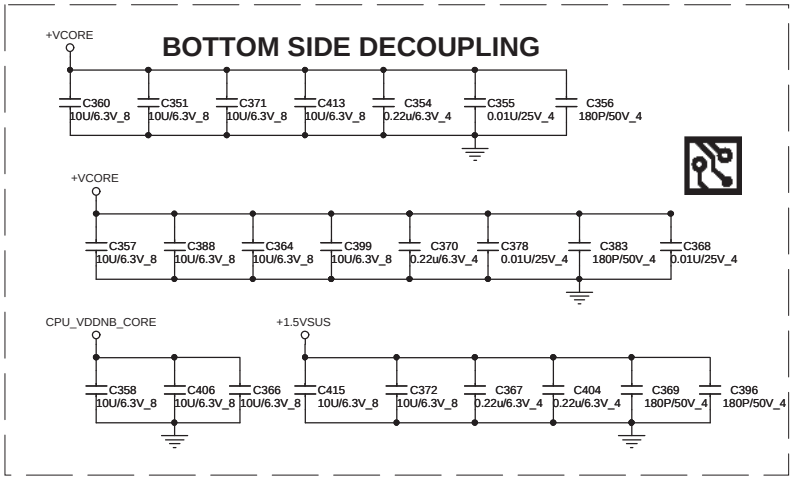
Size	Document Number	Rev
	S1G4 DDRIII MEMORY I/F 2/3	1A
Date: Wednesday, May 27, 2009	Sheet 3 of 49	

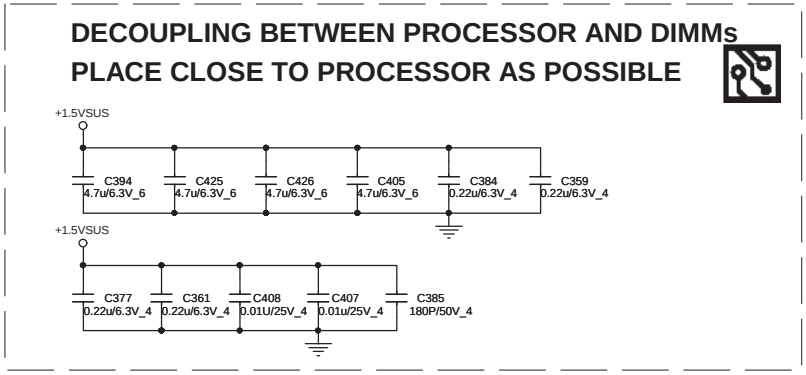
PROJECT : ZR8

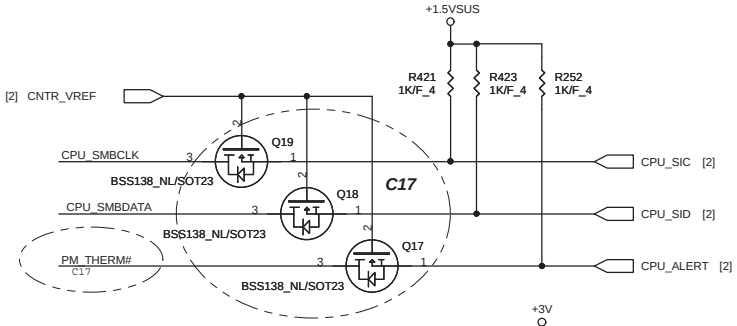
Quanta Computer Inc.



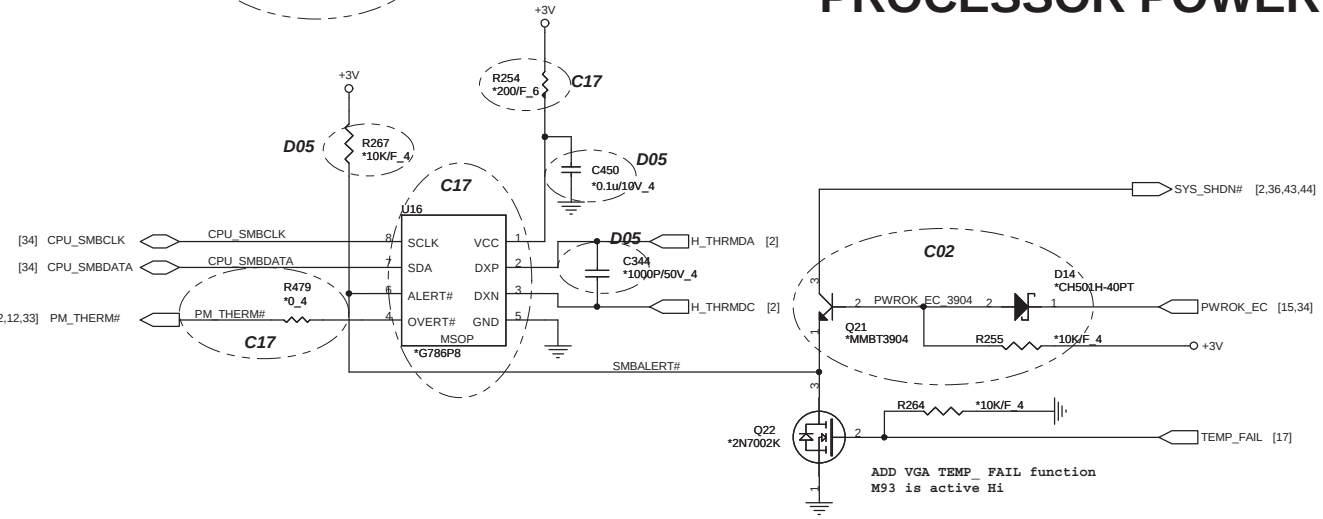








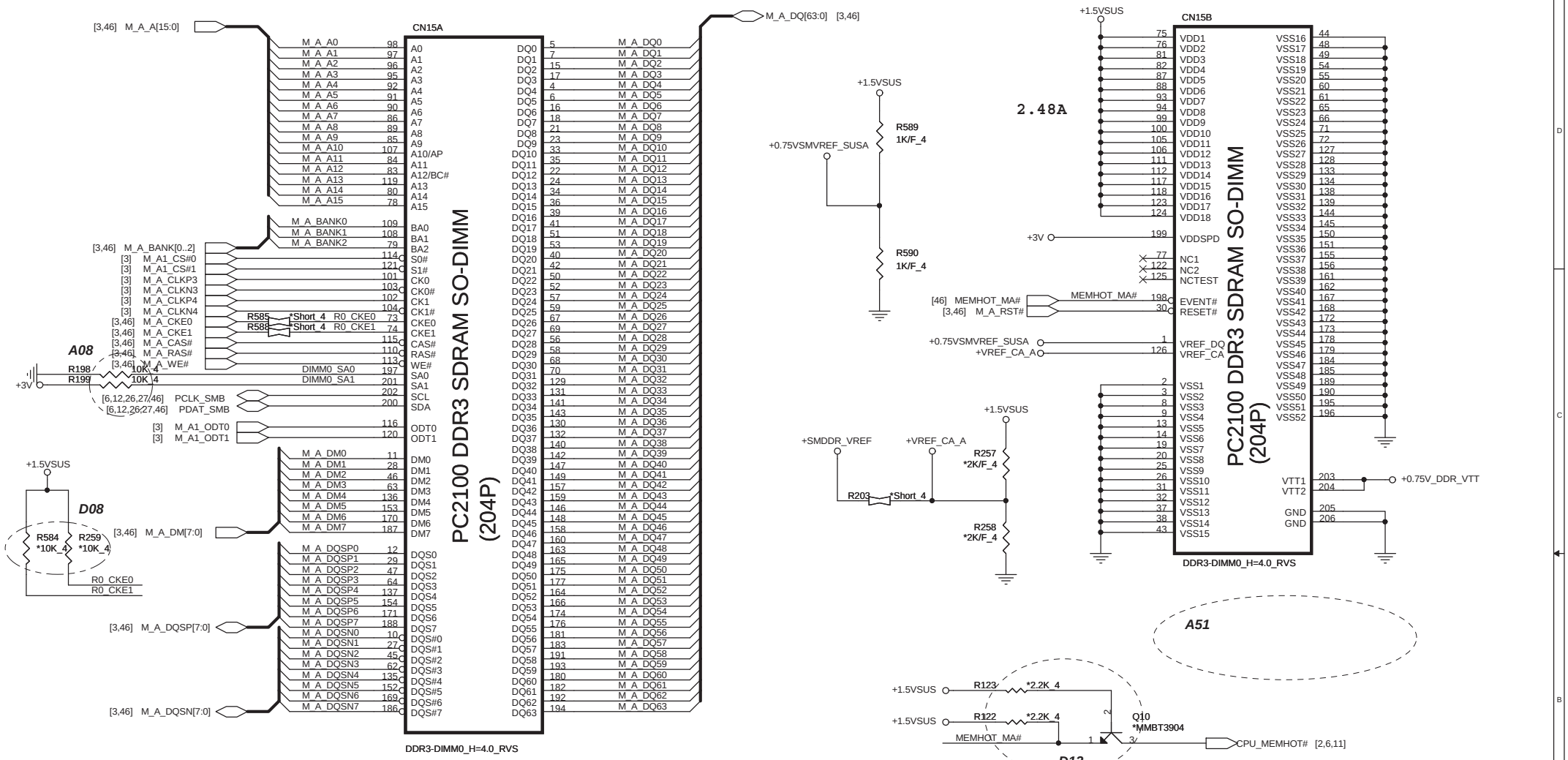
PROCESSOR POWER AND GROUND



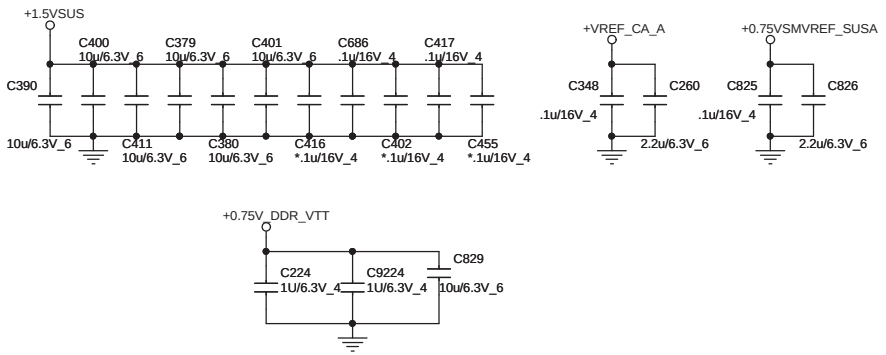
PROJECT : ZR8

Quanta Computer Inc.

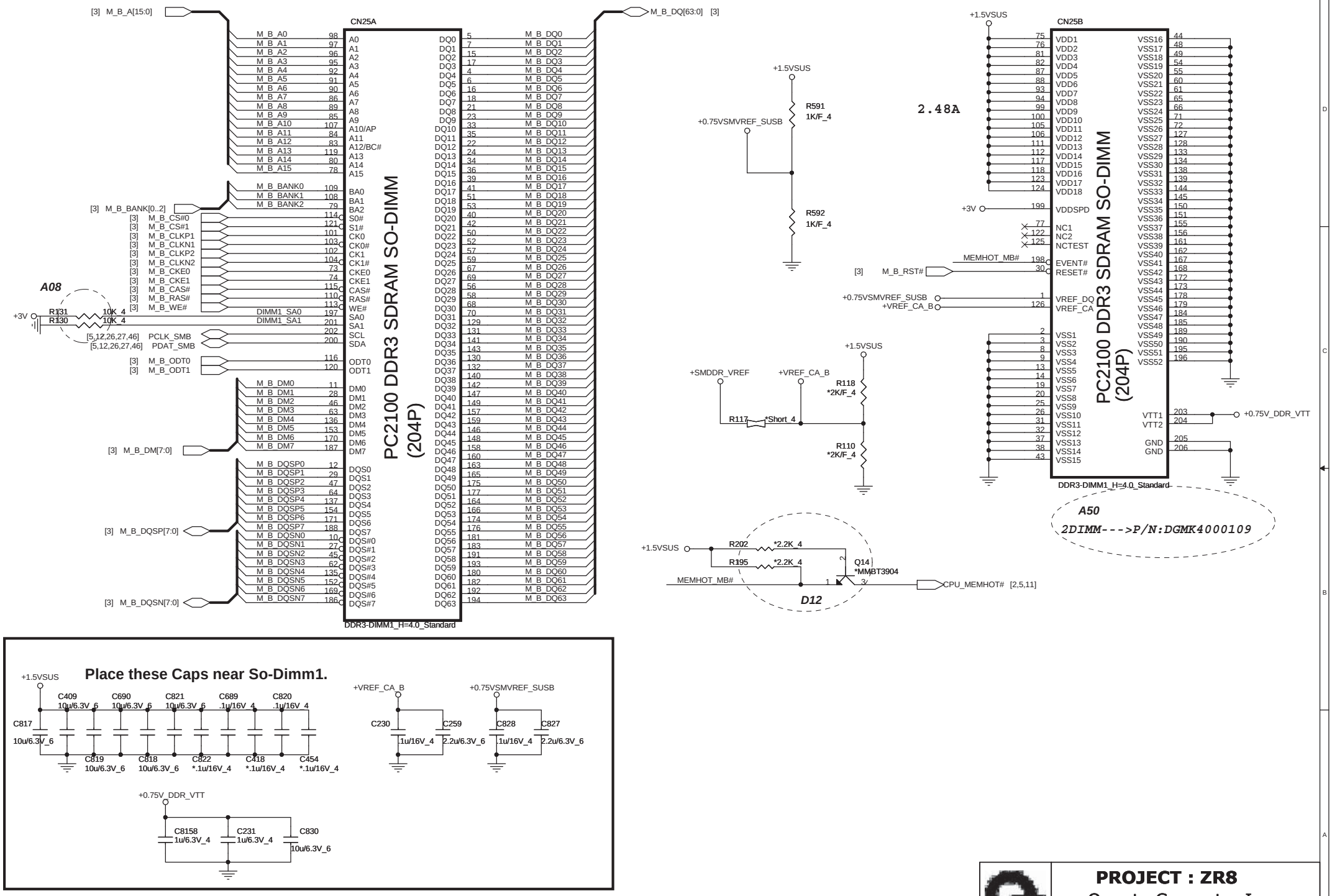
Size	Document Number	Rev
	S1G4 PWR & GND 3/3	1A
Date: Wednesday, May 27, 2009	Sheet 4 of 49	



Place these Caps near So-Dimm0.



PROJECT : ZR8		
Quanta Computer Inc.		
Size	Document Number: *DDR2 SODIMMS: A/B CHANNEL*	Rev 1A
Date: Wednesday, May 27, 2009	Sheet 5 of 49	


CN25A
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM1_H=4.0_Standard
[3] M_B_A[15:0]
M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14 M_B_A15
M_B_BANK0 M_B_BANK1 M_B_BANK2
[3] M_B_BANK[0..2]
[3] M_B_CS#0
[3] M_B_CS#1
[3] M_B_CLKP1
[3] M_B_CLKN1
[3] M_B_CLKP2
[3] M_B_CLKN2
[3] M_B_CKE0
[3] M_B_CKE1
[3] M_B_CAS#
[3] M_B_RAS#
[3] M_B_WE#
A08
+3V
R131 10K_4
R130 10K_4
DIMM1_SA0
DIMM1_SA1
[5,12,26,27,46] PCLK_SMB
[5,12,26,27,46] PDAT_SMB
[3] M_B_ODT0
[3] M_B_ODT1
M_B_DM0 M_B_DM1 M_B_DM2 M_B_DM3 M_B_DM4 M_B_DM5 M_B_DM6 M_B_DM7
[3] M_B_DM[7:0]
M_B_DQSP0 M_B_DQSP1 M_B_DQSP2 M_B_DQSP3 M_B_DQSP4 M_B_DQSP5 M_B_DQSP6 M_B_DQSP7
[3] M_B_DQSP[7:0]
M_B_DQSN0 M_B_DQSN1 M_B_DQSN2 M_B_DQSN3 M_B_DQSN4 M_B_DQSN5 M_B_DQSN6 M_B_DQSN7
[3] M_B_DQSN[7:0]
M_B_DQ[63:0] [3]
M_B_DQ0 M_B_DQ1 M_B_DQ2 M_B_DQ3 M_B_DQ4 M_B_DQ5 M_B_DQ6 M_B_DQ7 M_B_DQ8 M_B_DQ9 M_B_DQ10 M_B_DQ11 M_B_DQ12 M_B_DQ13 M_B_DQ14 M_B_DQ15 M_B_DQ16 M_B_DQ17 M_B_DQ18 M_B_DQ19 M_B_DQ20 M_B_DQ21 M_B_DQ22 M_B_DQ23 M_B_DQ24 M_B_DQ25 M_B_DQ26 M_B_DQ27 M_B_DQ28 M_B_DQ29 M_B_DQ30 M_B_DQ31 M_B_DQ32 M_B_DQ33 M_B_DQ34 M_B_DQ35 M_B_DQ36 M_B_DQ37 M_B_DQ38 M_B_DQ39 M_B_DQ40 M_B_DQ41 M_B_DQ42 M_B_DQ43 M_B_DQ44 M_B_DQ45 M_B_DQ46 M_B_DQ47 M_B_DQ48 M_B_DQ49 M_B_DQ50 M_B_DQ51 M_B_DQ52 M_B_DQ53 M_B_DQ54 M_B_DQ55 M_B_DQ56 M_B_DQ57 M_B_DQ58 M_B_DQ59 M_B_DQ60 M_B_DQ61 M_B_DQ62 M_B_DQ63
+1.5VSUS
R591 1K/F_4
+0.75VSMVREF_SUSB
R592 1K/F_4
2.48A
CN25B
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM1_H=4.0_Standard
+3V
MEMHOT_MB#
[3] M_B_RST#
+0.75VSMVREF_SUSB
+VREF_CA_B
VREF_DQ
VREF_CA
+0.75V_DDR_VTT
+SMDDR_VREF
+VREF_CA_B
R118 *2K/F_4
R117 *Short_4
R110 *2K/F_4
A50
2DIMM--->P/N:DGMK4000109
R202 *2.2K_4
R195 *2.2K_4
Q14 *MMBT3904
MEMHOT_MB#
CPU_MEMHOT# [2,5,11]
D12
Place these Caps near So-Dimm1.
C409 10u/6.3V_6
C690 10u/6.3V_6
C821 10u/6.3V_6
C689 .1u/16V_4
C820 .1u/16V_4
C817 10u/6.3V_6
C819 10u/6.3V_6
C818 10u/6.3V_6
C822 *.1u/16V_4
C418 *.1u/16V_4
C454 *.1u/16V_4
+VREF_CA_B
C230 .1u/16V_4
C259 2.2u/6.3V_6
+0.75VSMVREF_SUSB
C828 .1u/16V_4
C827 2.2u/6.3V_6
+0.75V_DDR_VTT
C8158 1u/6.3V_4
C231 1u/6.3V_4
C830 10u/6.3V_6
PROJECT : ZR8
Quanta Computer Inc.
Size
Document Number
DDR2 SODIMMS: A/B CHANNEL
Rev 1A
Date: Wednesday, May 27, 2009
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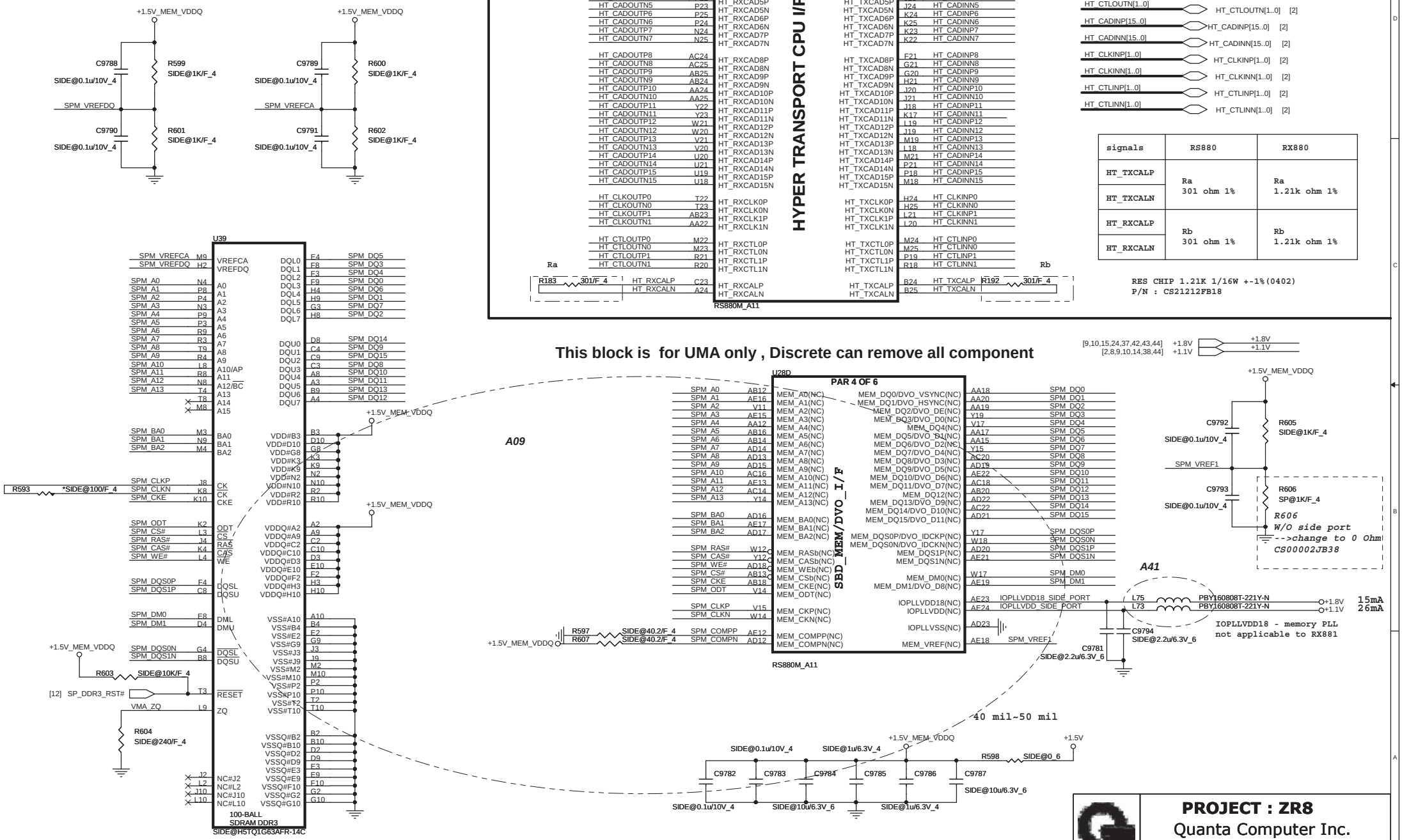
SIDE PORT

11/4



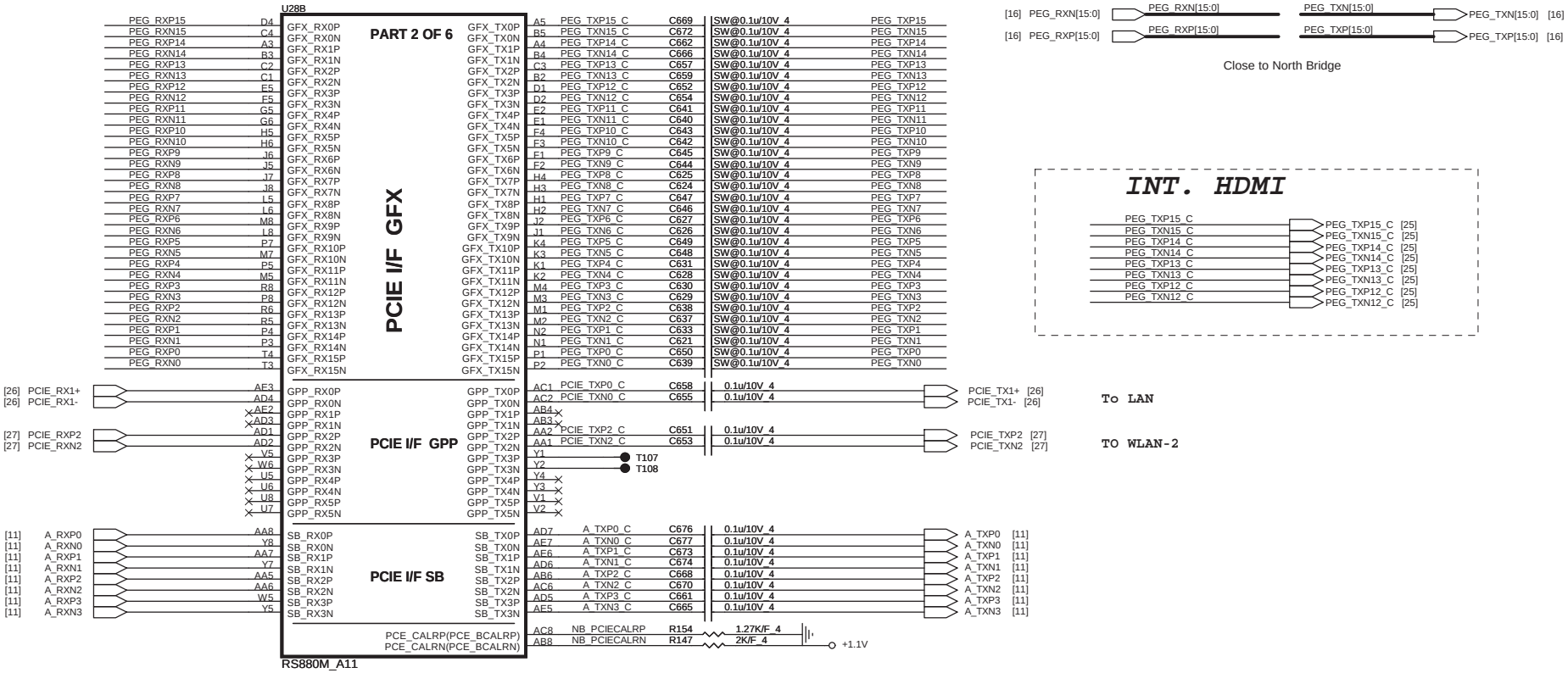
signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-HT LINK I/F 1/5	1A

Date: Wednesday, May 27, 2009 Sheet 7 of 49



RS880 Display Port Support (muxed on GFX)

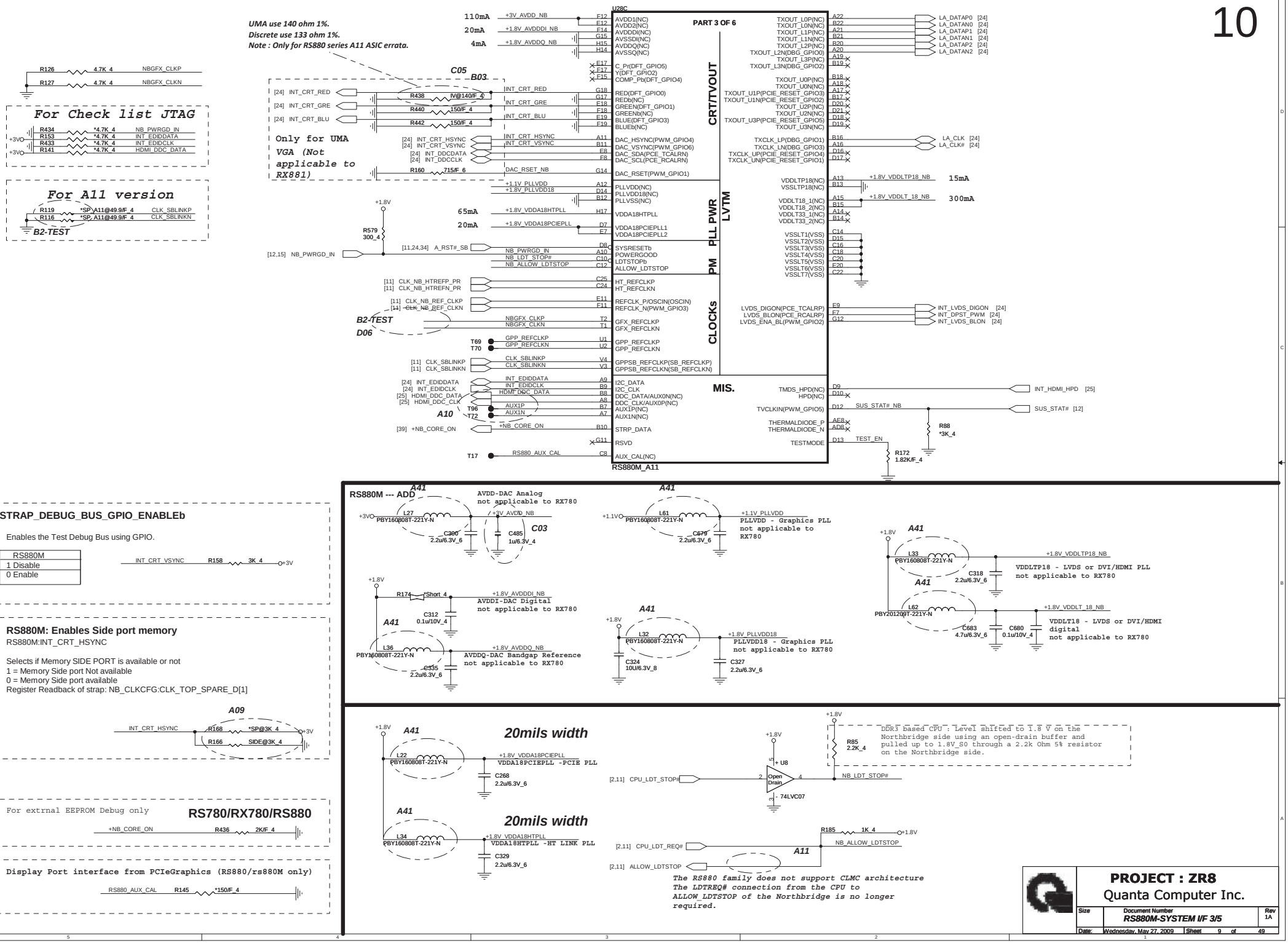
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-PCIE I/F 2/5	1A

Date: Wednesday, May 27, 2009 Sheet 8 of 49


UMA use 140 ohm 1%.
Discrete use 133 ohm 1%.
Note : Only for RS880 series A11 ASIC errata.
U28C
PART 3 OF 6
CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.
RS880M_A11
For Check list JTAG
For A11 version
B2-TEST
Only for UMA VGA (Not applicable to RX881)
B2-TEST D06
A10
C05
B03
C03
A41
A09
A11
RS880M --- ADD
AVDD-DAC Analog not applicable to RX780
PLLVDD - Graphics PLL not applicable to RX780
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780
AVDDI-DAC Digital not applicable to RX780
AVDDQ-DAC Bandgap Reference not applicable to RX780
PLLVDD18 - Graphics PLL not applicable to RX780
STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.
RS880M
1 Disable
0 Enable
RS880M: Enables Side port memory
RS880M:INT_CRT_HSYNC
Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
For extrnal EEPROM Debug only
RS780/RX780/RS880
Display Port interface from PCIeGraphics (RS880/rs880M only)
20mils width
VDDA18PCIEPLL -PCIE PLL
VDDA18HTPLL -HT LINK PLL
DDR3 based CPU : Level shifted to 1.8 V on the Northbridge side using an open-drain buffer and pulled up to 1.8V_S0 through a 2.2k Ohm 5% resistor on the Northbridge side.
The RS880 family does not support CLMC architecture The LDTREQ# connection from the CPU to ALLOW_LDTSTOP of the Northbridge is no longer required.
PROJECT : ZR8
Quanta Computer Inc.
Size
Document Number
RS880M-SYSTEM I/F 3/5
Rev 1A
Date: Wednesday, May 27, 2009
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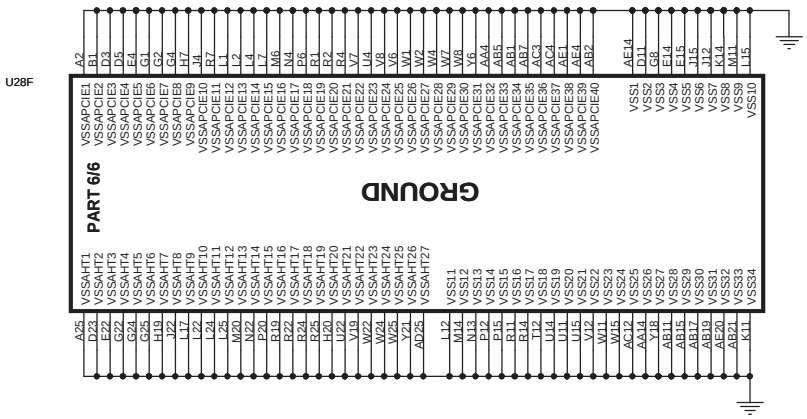
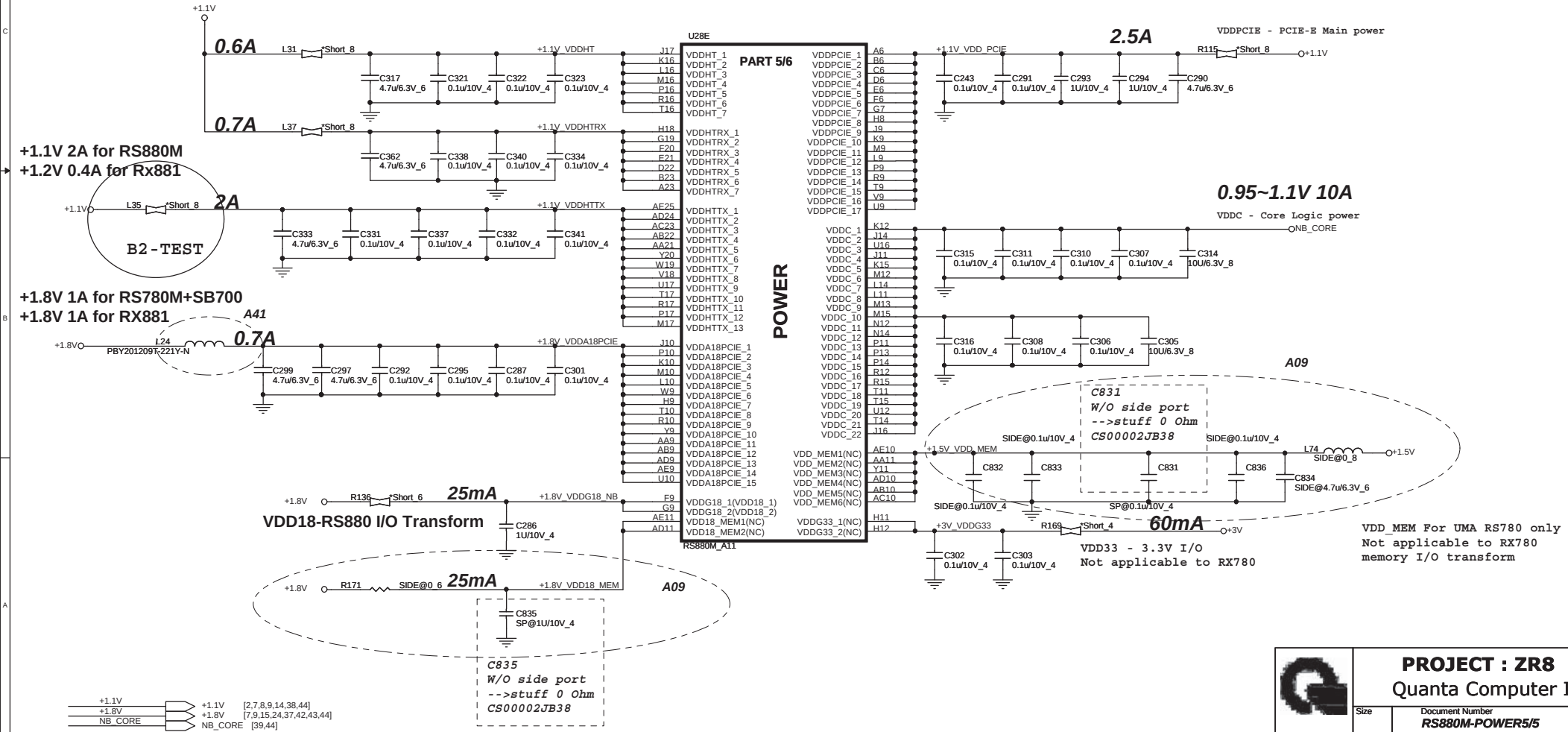


RX881/RS880 POWER DIFFERENCE TABLE

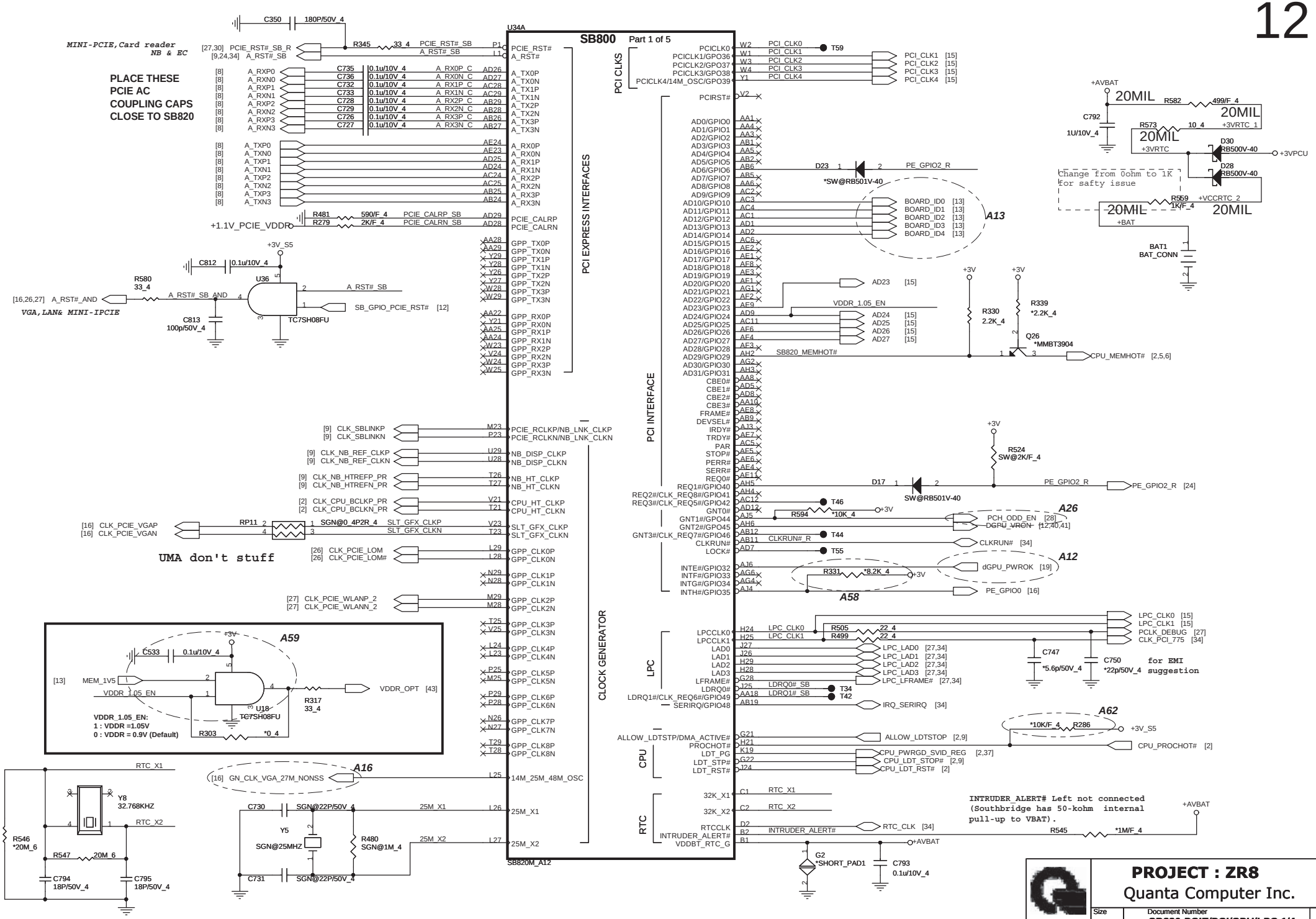
PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVDD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVDD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDLT18	GND	+1.8V
IOPLLVDD18	+1.8V	+1.8V	VDDLT33	NC	NC

+1.1V 2A for RS880M
+1.1V 1.3A for RX881



PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-POWER5/5	1A
Date: Wednesday, May 27, 2009	Sheet 10 of 49	


SB800 Part 1 of 5
U34A
MINI-PCIE,Card reader NB & EC
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB820
PCI EXPRESS INTERFACES
PCI CLKS
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
VGA,LAN& MINI-IPCIE
UMA don't stuff
VDDR_1.05_EN:
1 : VDDR =1.05V
0 : VDDR = 0.9V (Default)
Change from 0ohm to 1K for safty issue
for EMI suggestion
INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).
SB820M_A12
PROJECT : ZR8
Quanta Computer Inc.
SB820-PCIE/PCI/CPU/LPC 1/4
Rev 1A
Date: Wednesday, May 27, 2009
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NC only ,Can't be install

+3V_S5
R352 *2.2K_4 SB_TEST0
R350 *2.2K_4 SB_TEST1
R347 *2.2K_4 SB_TEST2

+3V
SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R288 2.2K_4 PCLK_SMB
R287 2.2K_4 PDAT_SMB

Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

+3V_S5
SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R348 10K_4 SB_SMBCLK1
R346 10K_4 SB_SMBDATA1

+3V_S5
SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R290 10K_4 SB_SCLK2
R283 10K_4 SB_SDATA2

+3V
R338 4.7K_4 SUS_STAT#

B2-TEST
+3V
R307 SW@4.7K_4
dGPU_VRON
2ms
MXM_PWR_EN
[19] MXM_PWREN
D19 SW@RB501V-40
MXM_PWR_EN
C538 SW@0.1u/10V_4
[11,40,41] DGPU_VRON
D18 *SW@RB501V-40
>1mS delay is required between all MXM power rail stable and MXM_PWREN(enables the module internal power)

A14

[11,13,14,15,24,26,31,32,36,44] +3V_S5 → +3V_S5
[2,4,5,6,9,10,11,13,14,15,19,24,25,27,29,30,32,33,34,36,37,38,39,41,42,43,44,46] +3V → +3V

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

U34D

SB800
Part 4 of 5

ACPI / WAKE UP EVENTS

Pin	Signal	Ext
J2	PCI_PME#/GEVENT4#	
K1	RI#/GEVENT22#	
D3	SPI_CS3#/GBE_STAT1/GEVENT21#	
E1	SLP_S3#	
H1	SLP_S5#	
F2	PWR_BTN#	[34] SUSB#
H5	PWR_GOOD	[34] SUSC#
G6	SUS_STAT#	[34] DNBSWON#
B3	TEST0	[15] SB_PWRGD_IN
C4	TEST1/TMS	[9] SUS_STAT#
F6	TEST2	SB_TEST0
AD21	GA20IN/GEVENT0#	SB_TEST1
AE21	KBRST#/GEVENT1#	SB_TEST2
K2	LPC_PME#/GEVENT3#	[34] SIO_A20GATE
J29	LPC_SMI#/GEVENT23#	[34] SIO_RCIN#
H2	GEVENT5#	T94 LANLINK_STATE#
J1	SYS_RESET#/GEVENT19#	[34] SIO_EXT_SMI#
H6	WAKE#/GEVENT8#	[34] SIO_EXT_SC#
E3	IR_RX1/GEVENT20#	T95 SYS_RST#
J6	THRMTRIP#/SMBALERT#/GEVENT2#	PCIE_WAKE#
AC19	NB_PWRGD	[26] PCIE_WAKE#
G1	RSMRST#	T58 IR_RX1
		SB_THERMTRIP#
		[2] CPU_THERMTRIP#
		[9,15] NB_PWRGD_IN
		[34] ICH_RSMRST#

USB 1.1 USB MISC

Pin	Signal	Ext
A10	USBCLK/14M_25M_48M_OSC	T106
G19	USB_RCOMP	USB_RCOMP_SB R293 11.8K/F_6
J10	USB_FSD1P/GPIO186	
H11	USB_FSD1N	
H9	USB_FSD0P/GPIO185	USB_FDS12P T47
J8	USB_FSD0N	USB_FSD12N T49

USB 2.0

Pin	Signal	Ext
B12	USB_HSD13P	USBP13+ [31]
A12	USB_HSD13N	USBP13- [31]
F11	USB_HSD12P	USBP12+ [31]
E11	USB_HSD12N	USBP12- [31]
E14	USB_HSD11P	
E12	USB_HSD11N	
J12	USB_HSD10P	USBP10+ [30]
J14	USB_HSD10N	USBP10- [30]
A13	USB_HSD9P	USBP9+ [31]
B13	USB_HSD9N	USBP9- [31]
D13	USB_HSD8P	USBP8+ [31]
C13	USB_HSD8N	USBP8- [31]
G12	USB_HSD7P	USBP7+ [27]
G14	USB_HSD7N	USBP7- [27]
G16	USB_HSD6P	T61
G18	USB_HSD6N	T105
D16	USB_HSD5P	
C16	USB_HSD5N	
B14	USB_HSD4P	
A14	USB_HSD4N	
E18	USB_HSD3P	
E16	USB_HSD3N	
J16	USB_HSD2P	
J18	USB_HSD2N	
B17	USB_HSD1P	USBP1+ [24]
A17	USB_HSD1N	USBP1- [24]
A16	USB_HSD0P	USBP0+ [31]
B16	USB_HSD0N	USBP0- [31]

USB board
USB board
USB card reader
BLUETOOTH
USB board
WLAN MINI CARD
USB CAMERA
On board USB connect
B2-TEST

GPIO

Pin	Signal	Ext
AD19	CLK_REQ4#/SATA_IS0#/GPIO64	
AA16	CLK_REQ3#/SATA_IS1#/GPIO63	
AB21	SMARTVOLT1/SATA_IS2#/GPIO50	
AC18	CLK_REQ0#/SATA_IS3#/GPIO60	
AF20	SATA_IS4#/FANOUT3/GPIO55	MXM_PWR_EN
AE19	SATA_IS5#/FANIN3/GPIO59	T37 SB_GPIO59
AF19	SPKR/GPIO66	[29] SPKR
AD22	SCL0/GPIO43	[5,6,26,27,46] PCLK_SMB
AF22	SDA0/GPIO47	[5,6,26,27,46] PDAT_SMB
E5	SCL1/GPIO227	SB_SMBCLK1
F4	SDA1/GPIO228	SB_SMBDATA1
AH21	CLK_REQ2#/FANIN4/GPIO62	[27] CLK_PCIE_2_REQ#
AB18	CLK_REQ1#/FANOUT4/GPIO61	R306 *0_4 [17] VGA_REQ# GPIO61
E1	IR_LED#/LLB#/GPIO184	C04
AJ21	SMARTVOLT2/SHUTDOWN#/GPIO51	
H4	DDR3_RST#/GEVENT7#	[7] SP_DDR3_RST#
D5	GBE_LED0/GPIO183	
D7	GBE_LED1/GEVENT9#	
G5	GBE_LED2/GEVENT10#	
K3	GBE_STAT0/GEVENT11#	
AA20	CLK_REQG#/GPIO65/OSCIN	T41

USB OC

Pin	Signal	Ext
H3	BLINK/USB_OC7#/GEVENT18#	[31] OC_7#
D1	USB_OC6#/IR_TX1/GEVENT6#	[31] OC_6#
E4	USB_OC5#/IR_TX0/GEVENT17#	R149 *Short_4 [2,4,33] PM_THERM#
D4	USB_OC4#/IR_RX0/GEVENT16#	[31] OC_4#
E8	USB_OC3#/AC_PRES/TDO/GEVENT15#	SB_JTAG_TDO
E7	USB_OC2#/TCK/GEVENT14#	SB_JTAG_TCK
E7	USB_OC1#/TDI/GEVENT13#	SB_JTAG_TDI
E8	USB_OC0#/TRST#/GEVENT12#	SB_JTAG_RST#

HD audio interface is +3VS5 voltage

HD AUDIO

Pin	Signal	Ext
M3	AZ_BITCLK	R555 *10K/F_4 ACZ_BCLK
N1	AZ_SDOUT	ACZ_SDOUT [15] ACZ_SDOUT
L2	AZ_SDIN0/GPIO167	R337 *10K/F_4 ACZ_SDIN0
M2	AZ_SDIN1/GPIO168	R336 *10K/F_4 ACZ_SDIN1
M1	AZ_SDIN2/GPIO169	R571 *10K/F_4 ACZ_SDIN2
M4	AZ_SDIN3/GPIO170	R327 *10K/F_4 ACZ_SDIN3
N2	AZ_SYNC	ACZ_SYNC
P2	AZ_RST#	ACZ_RST#

Pin	Signal	Ext
D25	SCL2/GPIO193	SB_SCLK2
F23	SDA2/GPIO194	SB_SDATA2
B26	SCL3_LV/GPIO195	SB_GPIO195
F26	SDA3_LV/GPIO196	SB_GPIO196
F25	EC_PWM0/EC_TIMER0/GPIO197	
F22	EC_PWM1/EC_TIMER1/GPIO198	
F22	EC_PWM2/EC_TIMER2/GPIO199	GPIO199 [15]
F21	EC_PWM3/EC_TIMER3/GPIO200	GPIO200 [15]

A61
+3V
R474 8.2K_4 CLK_PCIE_LAN_REQ#
R486 8.2K_4 CLK_PCIE_2_REQ#

+3V_S5
D03

GBE LAN

Pin	Signal	Ext
T1	GBE_COL	R653 10K_4 GBE_COL
T4	GBE_CRS	R322 10K_4 GBE_CRS
L6	GBE_MDCK	
L5	GBE_MDIO	R558 10K_4 GBE_MDIO
T9	GBE_RXCLK	
U1	GBE_RXD3	
U3	GBE_RXD2	
T2	GBE_RXD1	
U2	GBE_RXD0	
T5	GBE_RXCTL/RXDV	
V5	GBE_RXERR	R343 10K_4 GBE_RXERR
P5	GBE_TXCLK	
M5	GBE_TXD3	
P9	GBE_TXD2	
T7	GBE_TXD1	
P7	GBE_TXD0	
M7	GBE_TXCTL/TXEN	
P4	GBE_PHY_PD	
M9	GBE_PHY_RST#	
V7	GBE_PHY_INTR	R344 10K_4 GBE_PHY_INTR

EMBEDDED CTRL

Pin	Signal	Ext
F23	ADP_PRES0	T35
E24	PS2_DAT/SDA4/GPIO187	
E21	PS2_CLK/SCL4/GPIO188	
G29	SPI_CS2#/GBE_STAT2/GPIO166	
	FC_RST#/GPO160	
D27	PS2KB_DAT/GPIO189	
E28	PS2KB_CLK/GPIO190	
E29	PS2M_DAT/GPIO191	
E27	PS2M_CLK/GPIO192	

EMBEDDED CTRL

Pin	Signal
G24	KSI_0/GPIO201
G25	KSI_1/GPIO202
E28	KSI_2/GPIO203
E29	KSI_3/GPIO204
D29	KSI_4/GPIO205
D28	KSI_5/GPIO206
C29	KSI_6/GPIO207
C28	KSI_7/GPIO208
B28	KSO_0/GPIO209
A27	KSO_1/GPIO210
B27	KSO_2/GPIO211
D26	KSO_3/GPIO212
A26	KSO_4/GPIO213
C26	KSO_5/GPIO214
A24	KSO_6/GPIO215
B25	KSO_7/GPIO216
A25	KSO_8/GPIO217
D24	KSO_9/GPIO218
B24	KSO_10/GPIO219
C24	KSO_11/GPIO220
B23	KSO_12/GPIO221
A23	KSO_13/GPIO222
D22	KSO_14/GPIO223
C22	KSO_15/GPIO224
A22	KSO_16/GPIO225
B22	KSO_17/GPIO226

SB_GPIO195 R489 10K_4
SB_GPIO196 R275 10K_4

SB820M_A12

ACZ_SDOUT R570 33_4 ACZ_SDOUT_AUDIO [29]
C815 *10P/50V_4
ACZ_SYNC R552 33_4 ACZ_SYNC_AUDIO [29]
C800 *10P/50V_4
ACZ_BCLK R569 33_4 ACZ_BITCLK_AUDIO [29]
C814 *10P/50V_4
ACZ_RST# R554 33_4 ACZ_RST#_AUDIO [29]
ACZ_SDIN0 ACZ_SDIN0 [29]

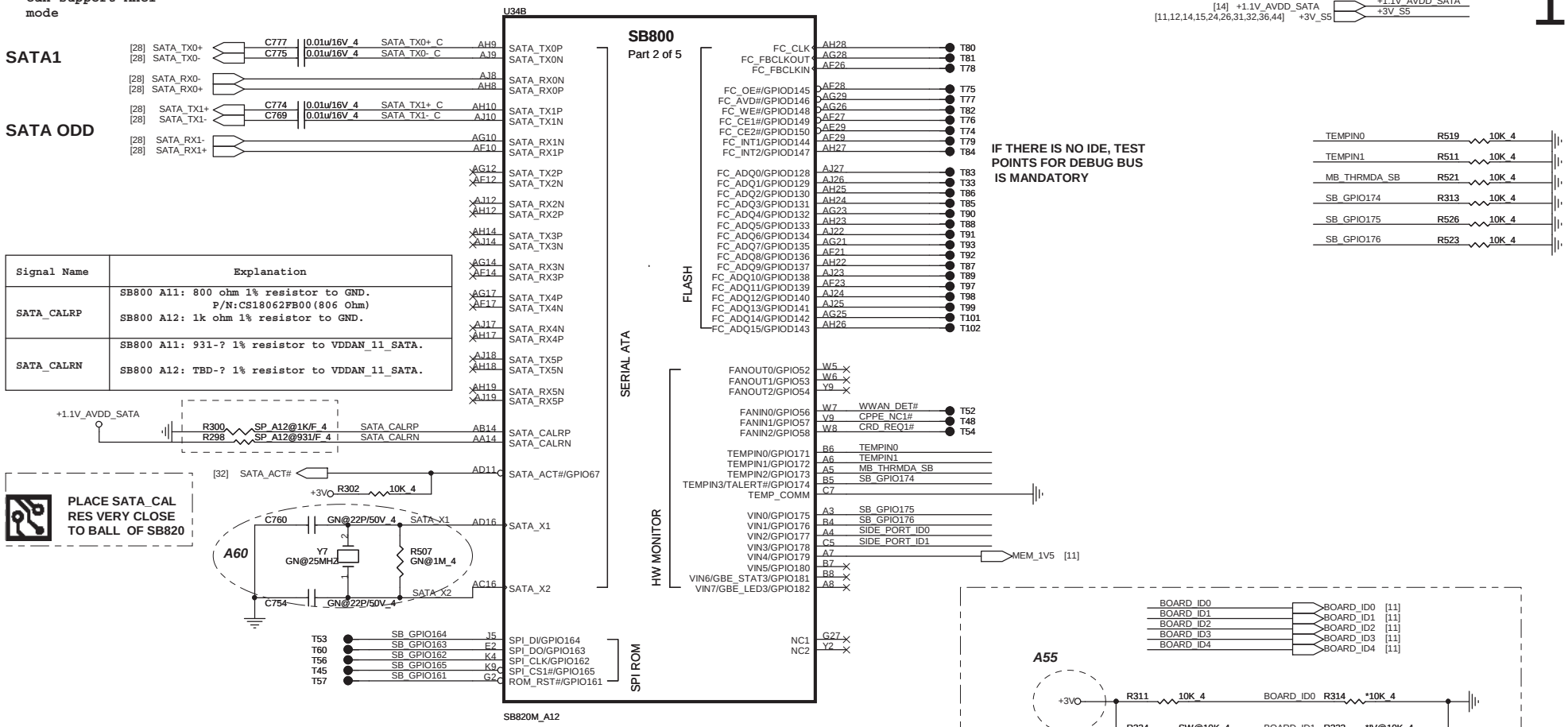
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

B2-TEST
CN24
+3V_S5
DEL C816
1 SB_JTAG_TCK
2 SB_JTAG_TDO
3 SB_JTAG_TDI
4 SB_TEST1
5
6 SB_JTAG_RST#
7
8
*S/W_JTAG_DEBUG
SB JTAG

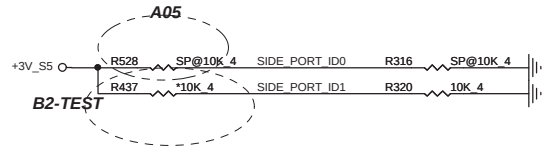
PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-ACPI/GPIO/USB 2/4	1A
Date: Wednesday, May 27, 2009	Sheet 12 of 49	

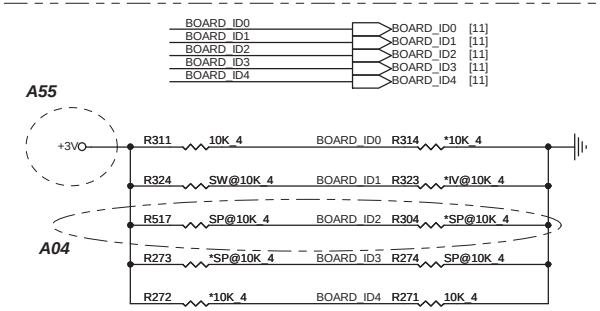
SATA PORT 0,1,2,3
can support AHCI
mode



Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. P/N:CS18062FB00(806 Ohm) SB800 A12: 1k ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931-? 1% resistor to VDDAN_11_SATA. SB800 A12: TBD-? 1% resistor to VDDAN_11_SATA.



	ID1	ID0
HYX	0	0
SAM	0	1
ATI	1	0



DDR3 Sideport Memory Device

Vendor	Vendor P/N	STN B/S P/N	Size	BOARD_ID2 GPIO12	SIDE_PORT_ID1 GPIO178	SIDE_PORT_ID0 GPIO177
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	0 (WO/Sideport)	0	0
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	1 (W/Sideport)	0	1

Board ID

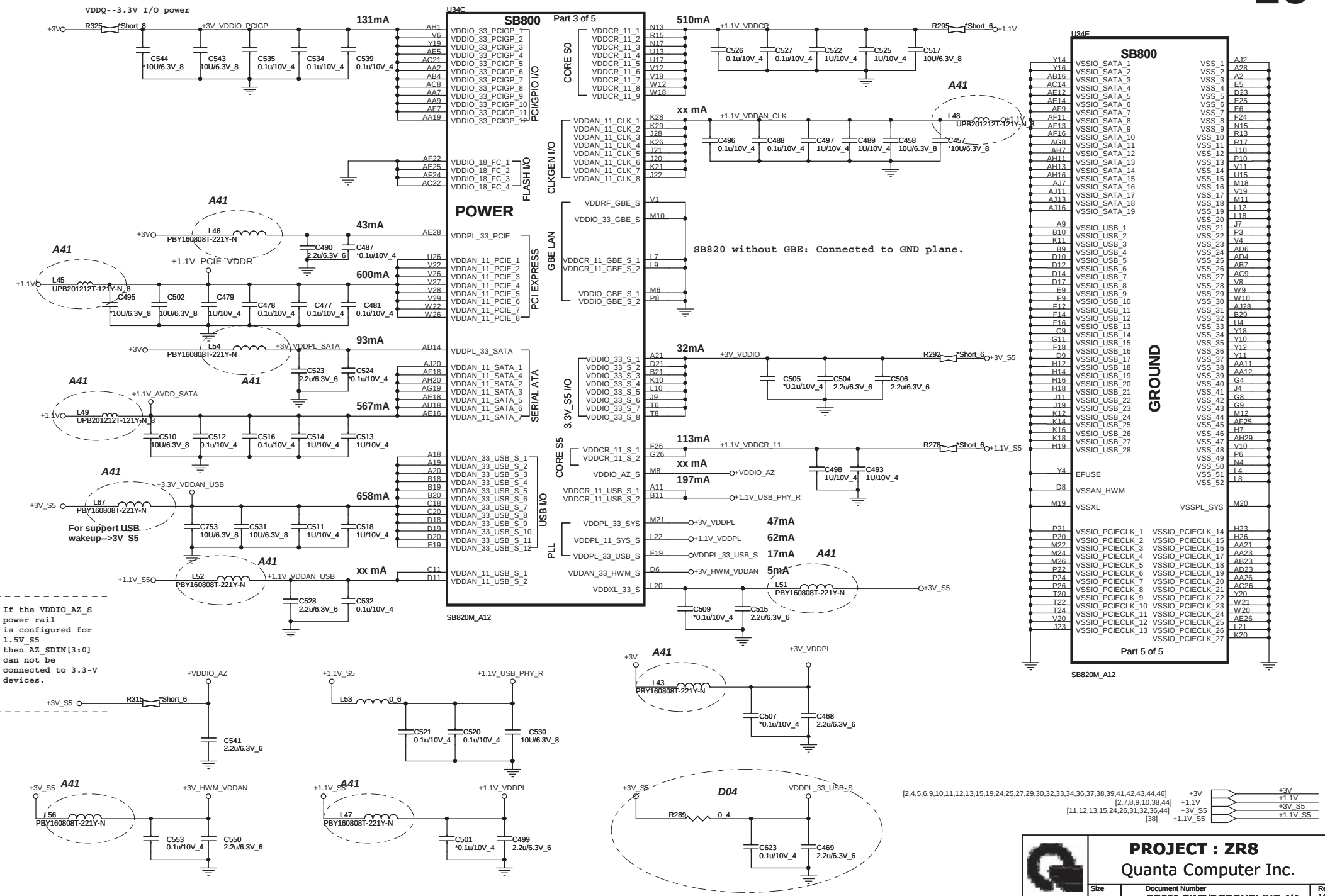
	BOARD_ID4 GPIO14	BOARD_ID3 GPIO13	BOARD_ID2 GPIO12	BOARD_ID1 GPIO11	BOARD_ID0 GPIO10
0	N/A (Default)	JV51-DN (3-DIMM) (Default)	WO/Sideport	UMA	14"
1	N/A	JM51-DN (2-DIMM)	W/Sideport (Default)	Discrete (Default)	15.6" (Default)

PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	SATA/IDE/HWM/SPI 3/4	1A

Date: Wednesday, May 27, 2009 Sheet 13 of 49

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.



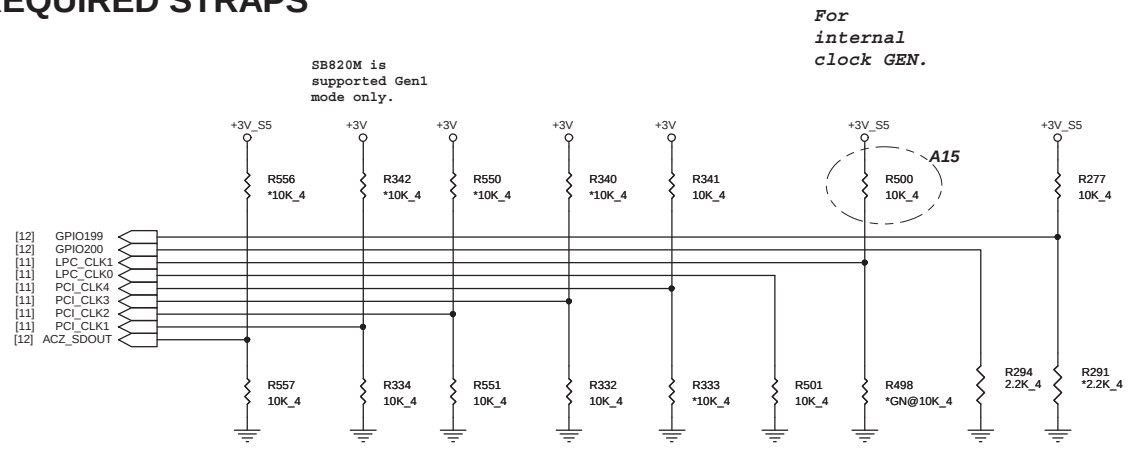
PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	SB820-PWR/DECOUPLING 4/4	1A
Date: Wednesday, May 27, 2009	Sheet 14 of 49	

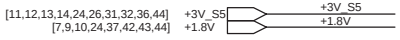
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS



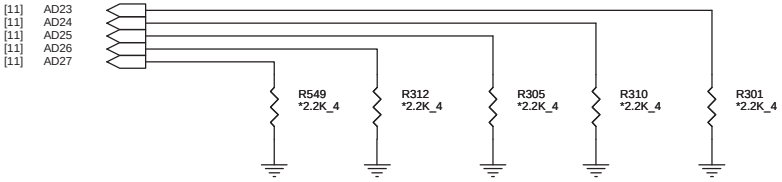
D02	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	This is required as the low power mode is not supported on the SB8xx	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	INT. CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	EXT. CLKGEN ENABLE	L,H=LPC ROM DEFAULT L, L=FWH ROM

internal have pull Hi 10K



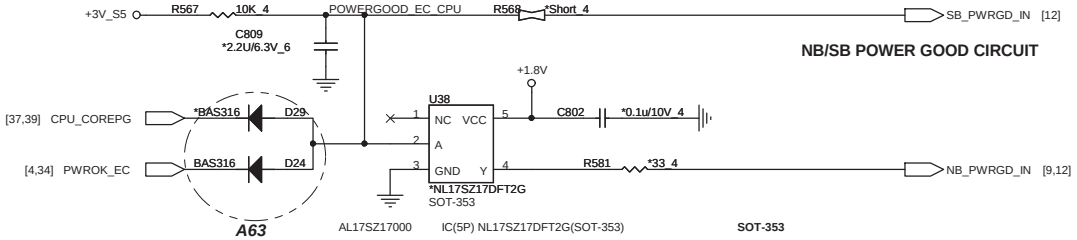
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE I2C ROM DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



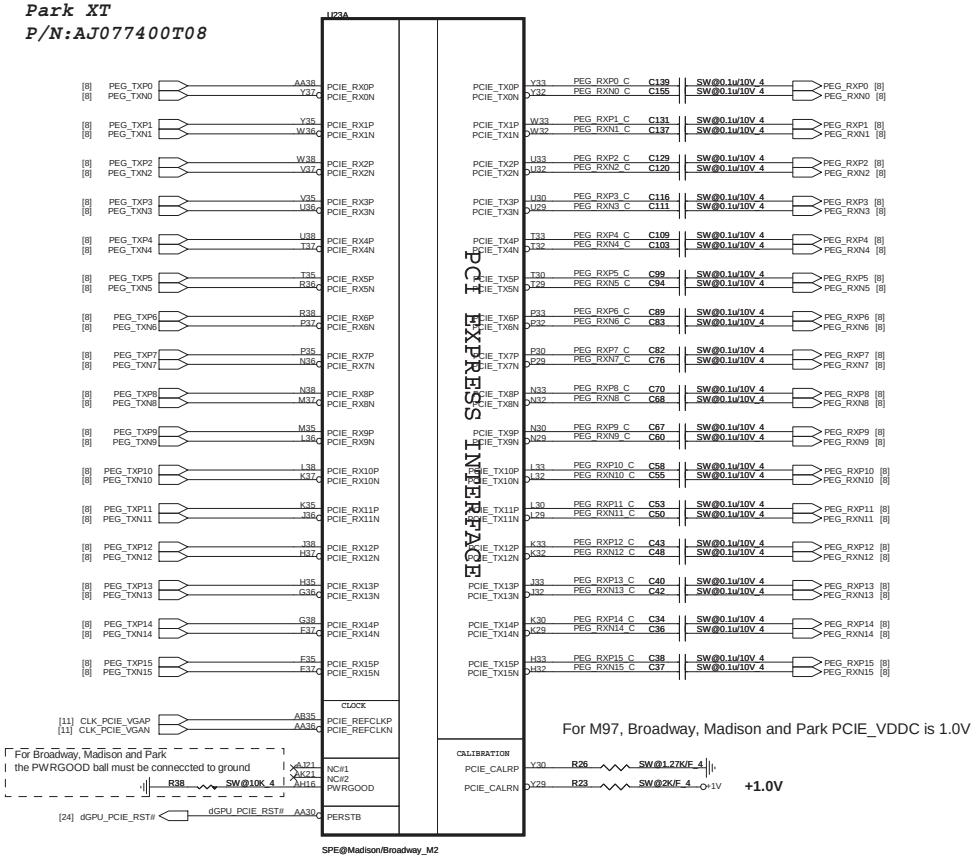
AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-STRAPS	1A

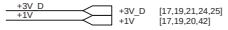
Date: Wednesday, May 27, 2009 Sheet 15 of 49

Park XT
P/N:AJ077400T08

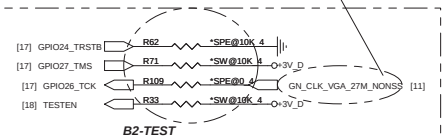


For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

+1.0V

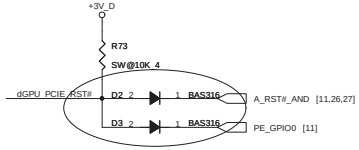


Add extra OSC for use SB clock.



JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBUG)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
TESTEN	"1" (PU)	"1" (PU)



B2-TEST
FORM RB501 CHANGE TO BAS316

PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	Madison/Broadway-PCIE I/F	1A

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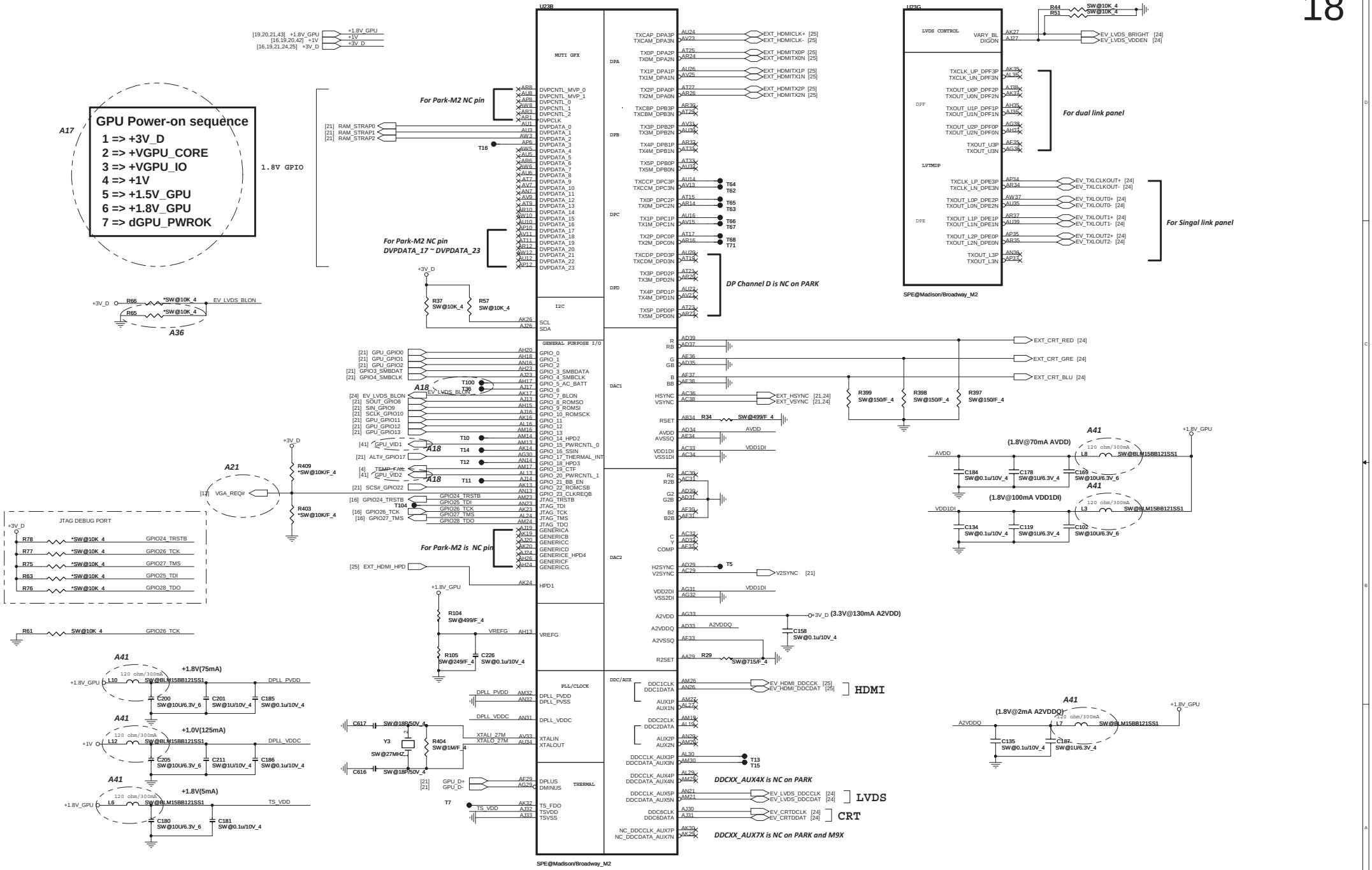
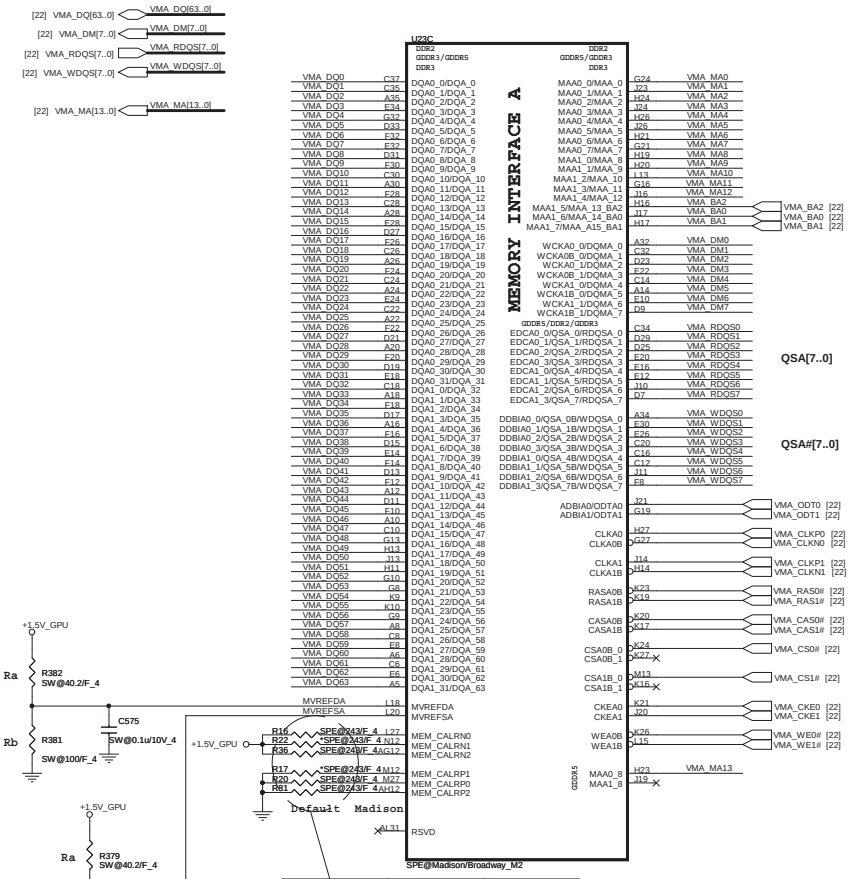
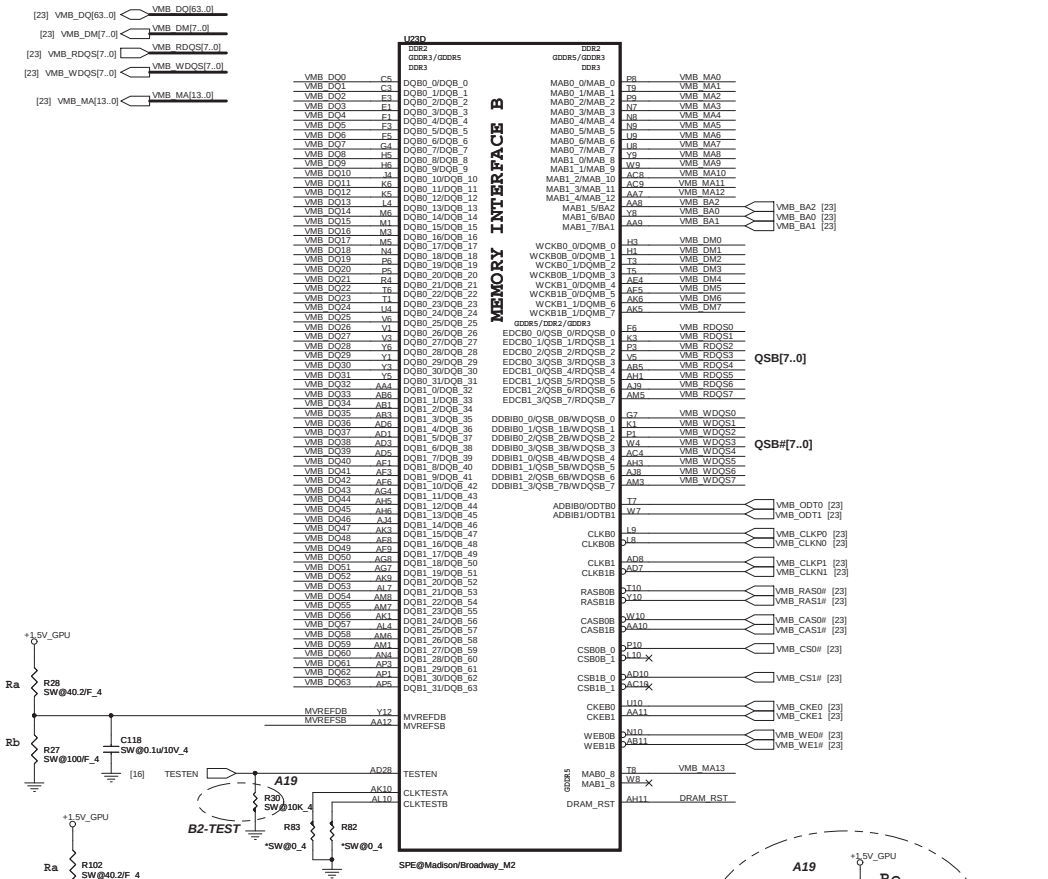
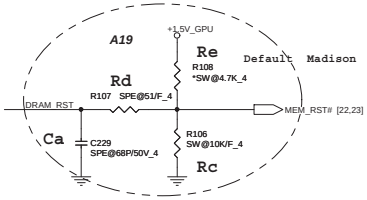

GPU Power-on sequence
1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK
A17
U23B
MUTI GFX
DPA
DPB
DPC
DPD
I2C
GENERAL PURPOSE I/O
DAC1
DAC2
DDC/AUX
PLL/CLOCK
THERMAL
For Park-M2 NC pin
For Park-M2 NC pin
DVPDATA_17 ~ DVPDATA_23
DP Channel D is NC on PARK
For Park-M2 is NC pin
HDMI
LVDS
CRT
DDCXX_AUX4X is NC on PARK
DDCXX_AUX7X is NC on PARK and M9X
SPE@Madison/Broadway_M2
U23G
LVDS CONTROL
LVTMDP
DPF
DPE
For dual link panel
For Singal link panel
SPE@Madison/Broadway_M2
A36
A21
A18
A41
(1.8V@70mA AVDD)
(1.8V@100mA VDD1DI)
(1.8V@2mA A2VDDQ)
+1.8V(75mA)
+1.0V(125mA)
+1.8V(5mA)
(3.3V@130mA A2VDD)
JTAG DEBUG PORT
PROJECT : ZR8
Quanta Computer Inc.
Madison/Broadway-HOST I/F
Wednesday, May 27, 2009
Sheet 17 of 49



	For PARK	For Madison
MEM_CALRNP0		stuff
MEM_CALRNP1	stuff	
MEM_CALRNP2		stuff

For M97,Broadway,madison & PARK only.





DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3(Default)
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

Broadway no daul rank support for GDDR5

+1.5V_GPU → +1.5V_GPU [19,22,23,40,43]

Designator	For M97-M2	For Mannhatton
Rc	10K	10K
Rd	0R/Short	51R
Re	DNI	DNI
Ca	2.2nF	68pF

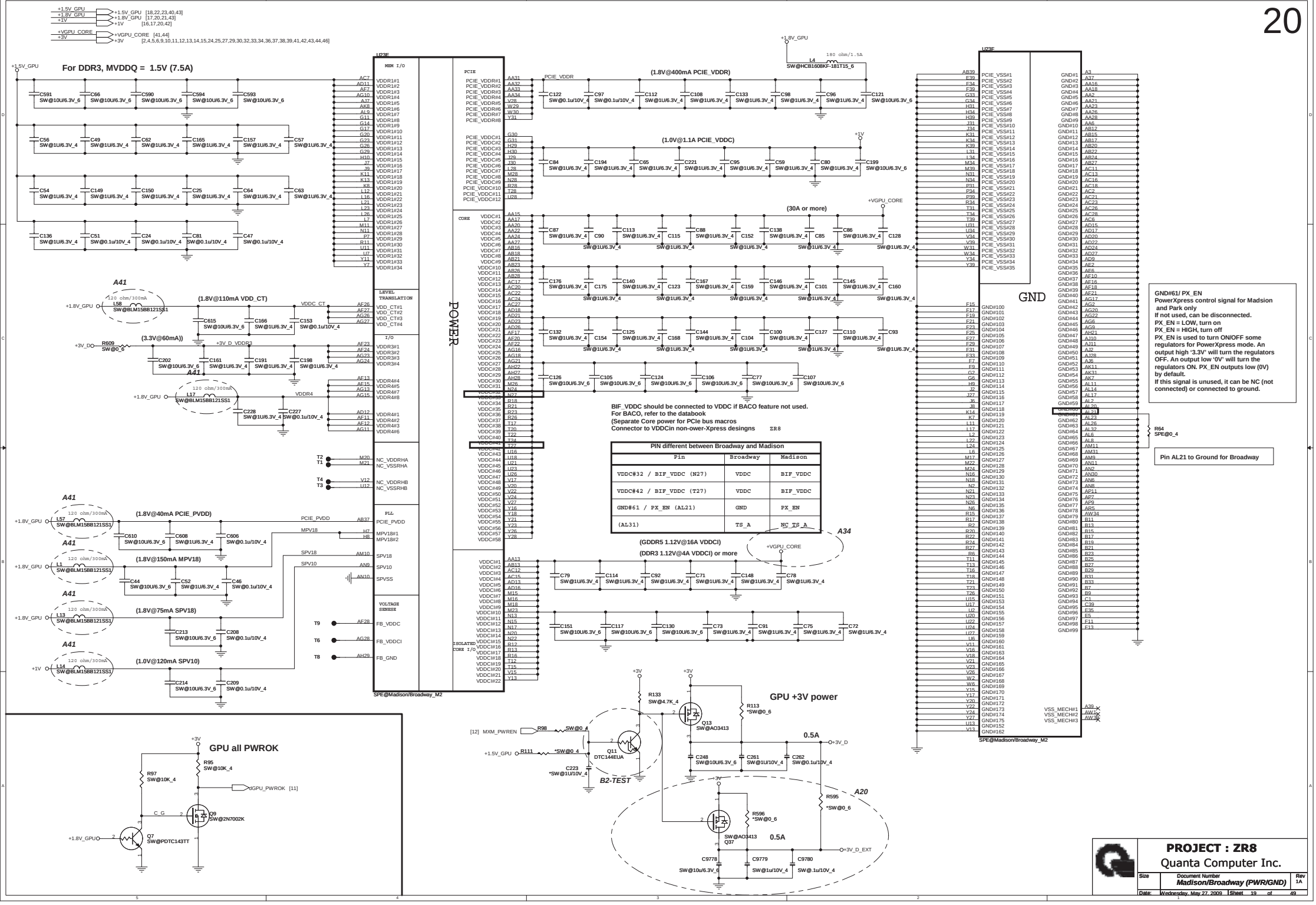
This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

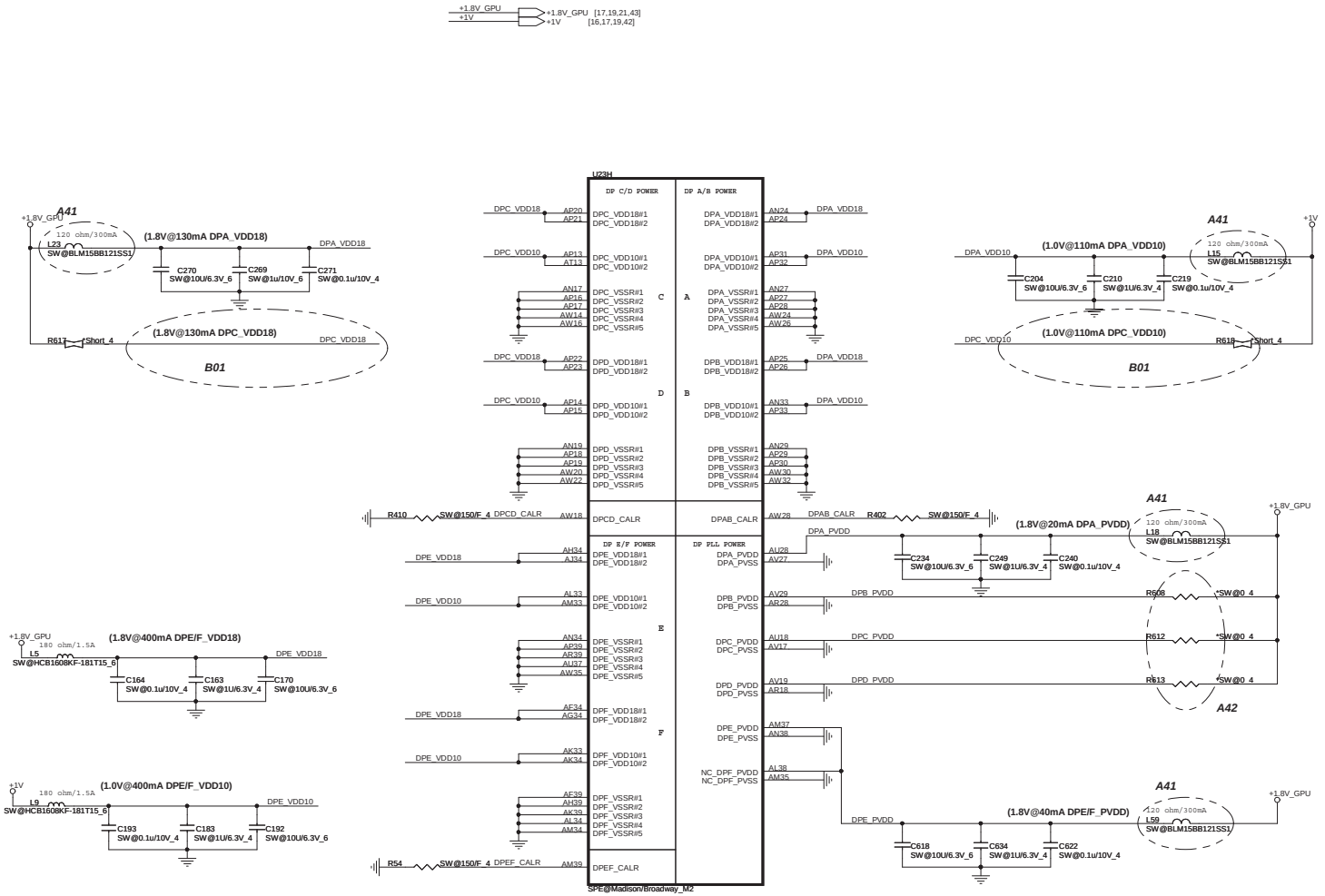
PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	Madison/Broadway-MEM I/F	1A

Date: Wednesday, May 27, 2009 Sheet 18 of 49


+1.5V_GPU
+1.8V_GPU
+1V
+1.5V_GPU [18,22,23,40,43]
+1.8V_GPU [17,20,21,43]
+1V [16,17,20,42]
+VGPU_CORE
+3V
+VGPU_CORE [41,44]
+3V [2,4,5,6,9,10,11,12,13,14,15,24,25,27,29,30,32,33,34,36,37,38,39,41,42,43,44,46]
For DDR3, MVDDQ = 1.5V (7.5A)
U23E
POWER
MEM I/O
PCIE
CORE
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENSE
ISOLATED CORE I/O
SPE@Madison/Broadway_M2
(1.8V@400mA PCIE_VDDR)
(1.0V@1.1A PCIE_VDDC)
(30A or more)
(1.8V@110mA VDD_CT)
(3.3V@60mA))
(1.8V@40mA PCIE_PVDD)
(1.8V@150mA MPV18)
(1.8V@75mA SPV18)
(1.0V@120mA SPV10)
A41
BIF_VDDC should be connected to VDDC if BACO feature not used.
For BACO, refer to the databook
(Separate Core power for PCIe bus macros
Connector to VDDCin non-ower-Xpress designs ZR8
PIN different between Broadway and Madison
Pin | Broadway | Madison
VDDC#32 / BIF_VDDC (N27) | VDDC | BIF_VDDC
VDDC#42 / BIF_VDDC (T27) | VDDC | BIF_VDDC
GND#61 / PX_EN (AL21) | GND | PX_EN
(AL31) | TS_A | NC_TS_A
(GDDR5 1.12V@16A VDDCI)
(DDR3 1.12V@4A VDDCI) or more
A34
GPU +3V power
0.5A
B2-TEST
A20
U23F
GND
GND#61/ PX_EN
PowerXpress control signal for Madsion and Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high '3.3V' will turn the regulators OFF. An output low '0V' will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.
R64 SPE@0_4
Pin AL21 to Ground for Broadway
GPU all PWROK
PROJECT : ZR8
Quanta Computer Inc.
Size
Document Number
Madison/Broadway (PWR/GND)
Rev 1A
Date: Wednesday, May 27, 2009
Sheet 19 of 49



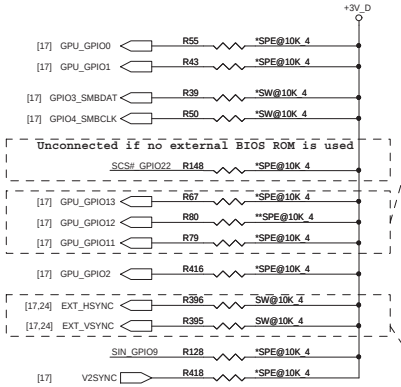
PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	Madison/Broadway (DP_PWR/GND)	1A

Date: Wednesday, May 27, 2009 Sheet 20 of 49

PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

Function Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

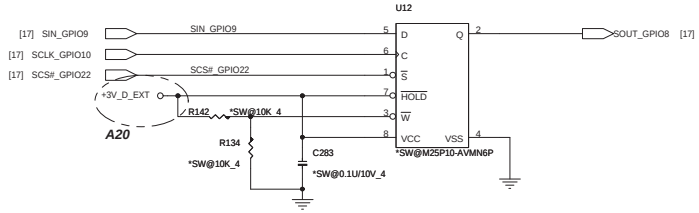
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

ZR8

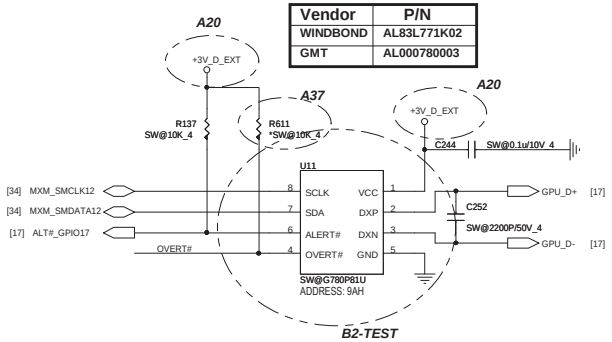
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	(Recommended setting as 5.0 GT/s capability will be controlled by software.)
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable 1 = VGA controller capacity disenable (The device will not be recognized as the system's VGA controller.)	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET. 1 = DRIVER would use the value sample on VHAD_0 during RESET.	0	

SERIAL ROM



Thermal Sensor

Vendor	P/N
WINDBOND	AL83L771K02
GMT	AL000780003

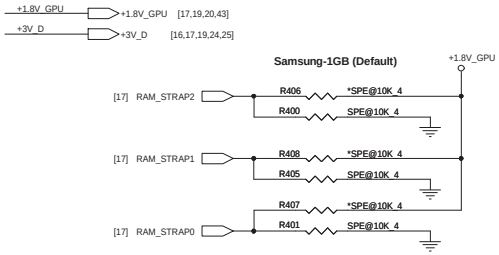


DDR3 Memory Aperture size

DDR3 Memory Aperture size

Vendor	Vendor P/N	STN B/S P/N	GPU	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			Park	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	Madison	1	0	0
			2Gb	1	1	1
Samsung			Park	0	1	0
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	Madison	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2Gb	0	0	1
AMD			Park	0	1	1
	23EY2387MA12-SZ	AKD5LGGT700	Madison	1	0	1

C14
D10



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

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Quanta Computer Inc.

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	Strip/Thermal	1A

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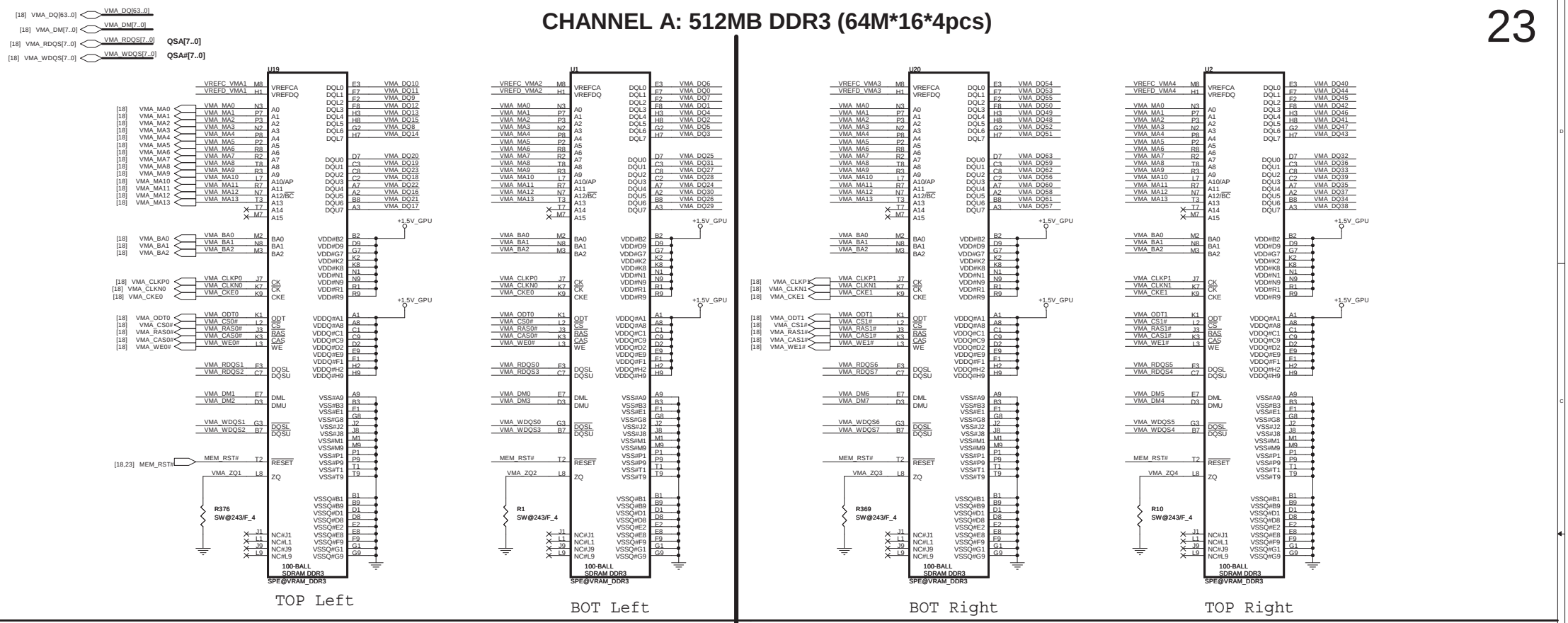
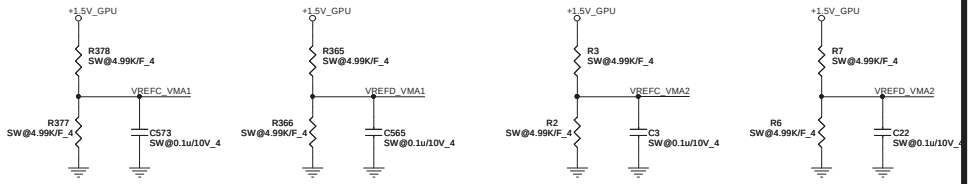
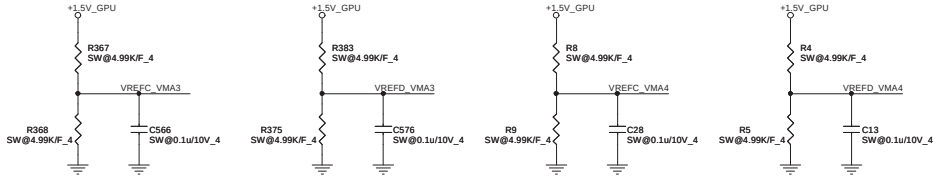
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



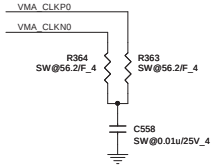
Group-A0 VREF



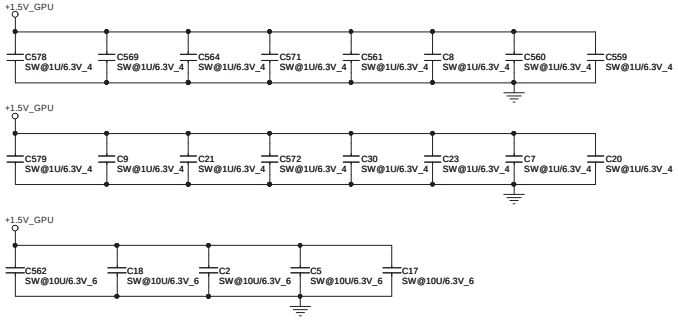
Group-A1 VREF



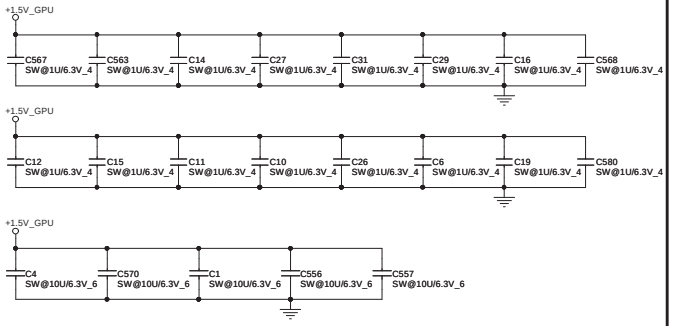
MEM_A0 CLK



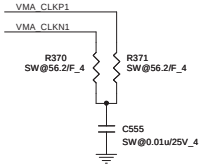
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



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Quanta Computer Inc.

Size	Document Number	Rev
	MEMORY 1 channel A	1A

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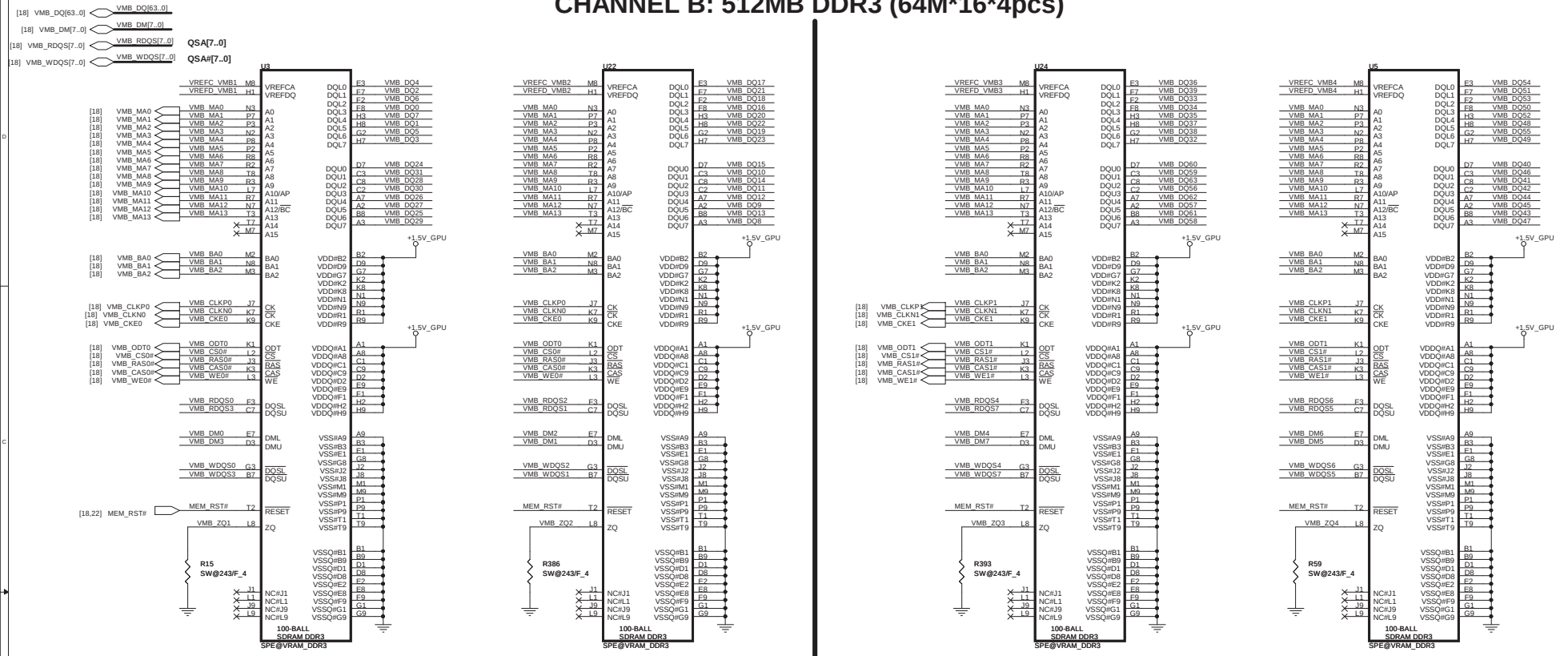
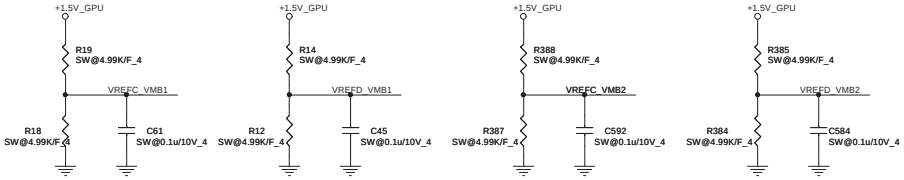
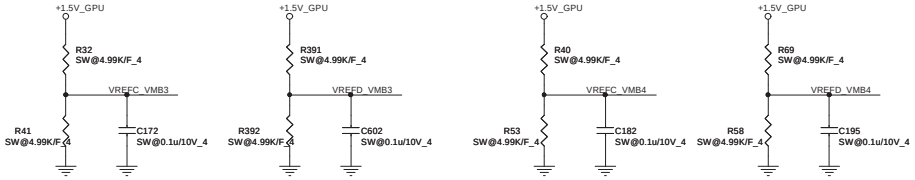
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



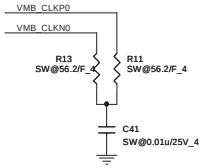
Group-B0 VREF



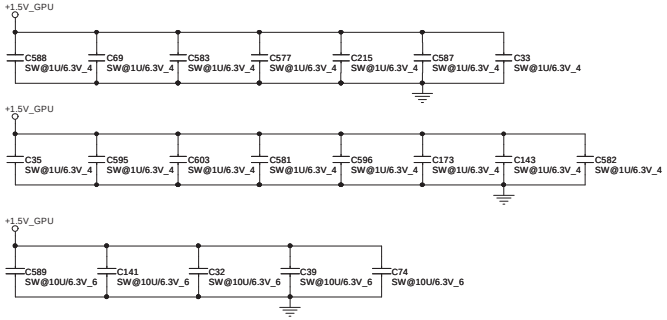
Group-B1 VREF



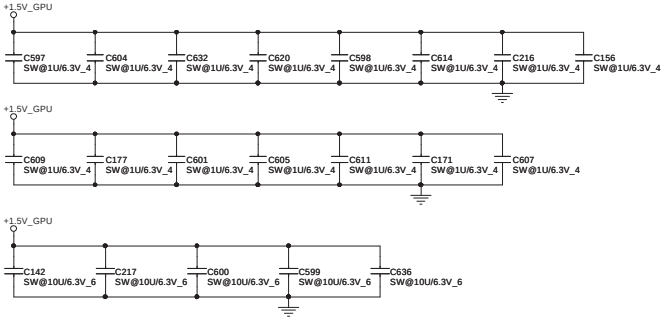
MEM_B0 CLK



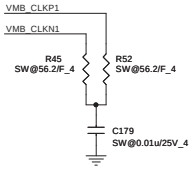
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



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Quanta Computer Inc.

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	MEMORY 2 channel B	1A

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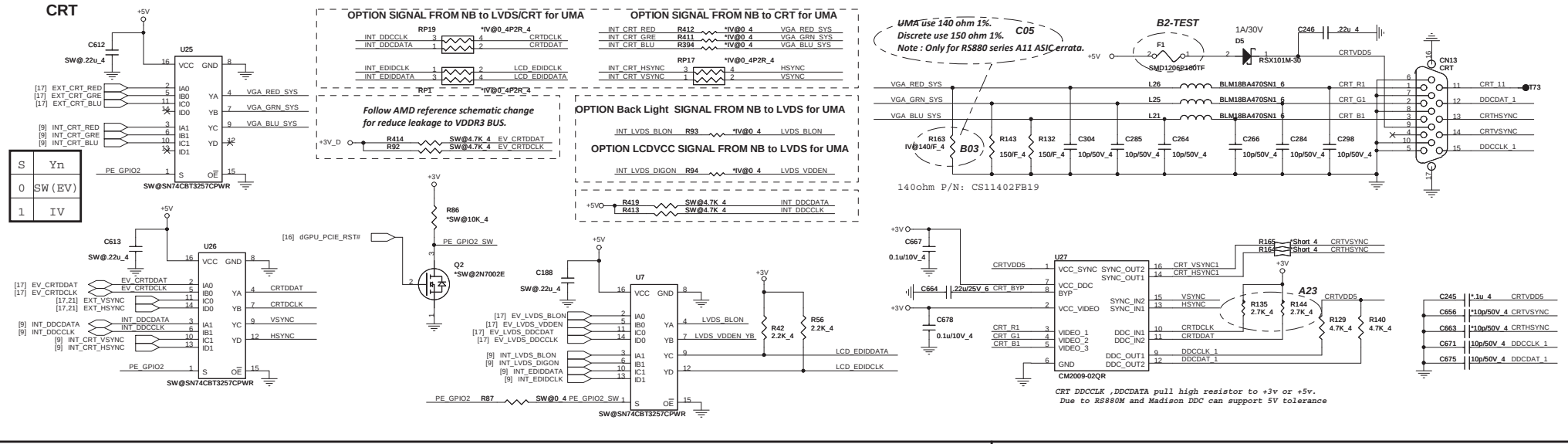
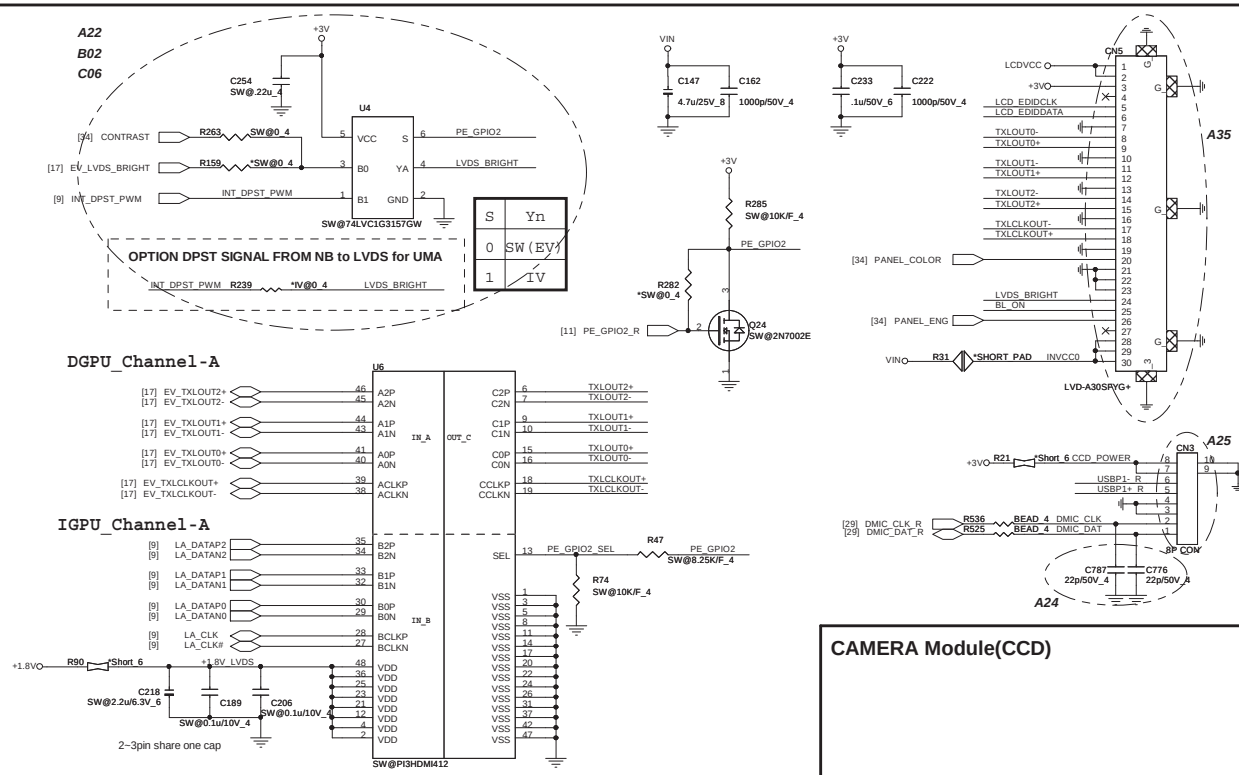
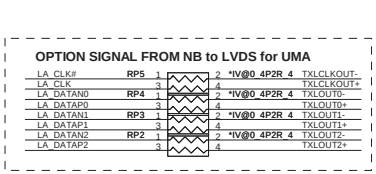
CRT



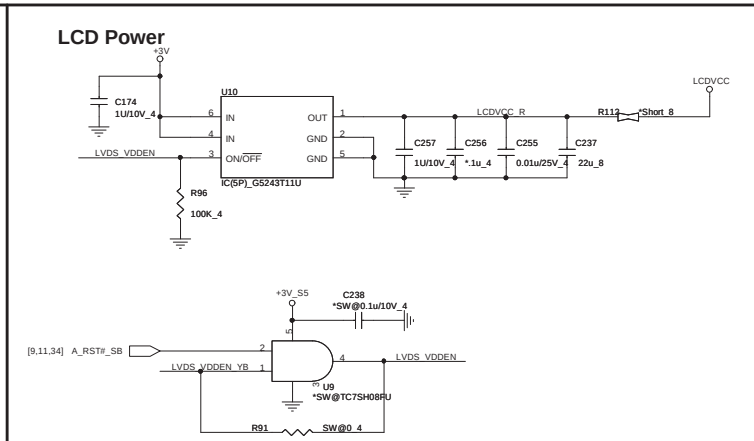
S	Yn
0	SW(EV)
1	IV



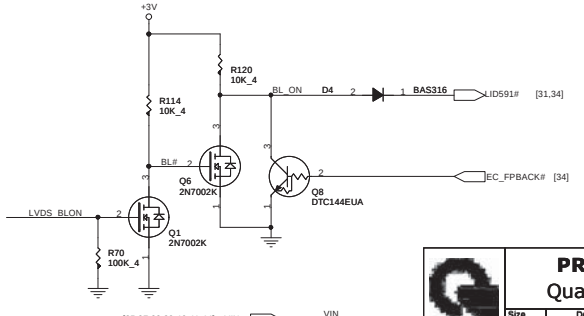
PE_GPIO2	Output
L	EV_LVDS
H	INT_LVDS



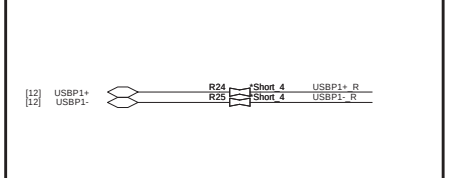
LCD Power



Backlight Control



CAMERA Module(CCD)



PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	CRT/LVDS/LID	1A
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UMA/DISCRETE select for HDMI

From RS880M

for Layout concern ,placement close north bridge

for Layout concern ,placement close HDMI conn

[8] PEG_TXN15_C	C280	*IV@0.1U/10V_4	TX2_HDMI-L	RP10	*IV@0_4P2R_4	TX2_HDMI-
[8] PEG_TXP15_C	C272	*IV@0.1U/10V_4	TX2_HDMI+L			TX2_HDMI+
[8] PEG_TXN14_C	C267	*IV@0.1U/10V_4	TX1_HDMI-L	RP9	*IV@0_4P2R_4	TX1_HDMI-
[8] PEG_TXP14_C	C263	*IV@0.1U/10V_4	TX1_HDMI+L			TX1_HDMI+
[8] PEG_TXN13_C	C253	*IV@0.1U/10V_4	TX0_HDMI-L	RP8	*IV@0_4P2R_4	TX0_HDMI-
[8] PEG_TXP13_C	C247	*IV@0.1U/10V_4	TX0_HDMI+L			TX0_HDMI+
[8] PEG_TXN12_C	C239	*IV@0.1U/10V_4	TXC_HDMI-L	RP7	*IV@0_4P2R_4	TXC_HDMI-
[8] PEG_TXP12_C	C232	*IV@0.1U/10V_4	TXC_HDMI+L			TXC_HDMI+

From dGPU

[17] EXT_HDMITX2N	C698	SW@0.1u/10V_4	TX2_HDMI-
[17] EXT_HDMITX2P	C697	SW@0.1u/10V_4	TX2_HDMI+
[17] EXT_HDMITX1N	C696	SW@0.1u/10V_4	TX1_HDMI-
[17] EXT_HDMITX1P	C695	SW@0.1u/10V_4	TX1_HDMI+
[17] EXT_HDMITX0N	C694	SW@0.1u/10V_4	TX0_HDMI-
[17] EXT_HDMITX0P	C693	SW@0.1u/10V_4	TX0_HDMI+
[17] EXT_HDMICLK-	C692	SW@0.1u/10V_4	TXC_HDMI-
[17] EXT_HDMICLK+	C691	SW@0.1u/10V_4	TXC_HDMI+

for Layout concern ,placement close HDMI conn

+5V, Q34 2N7002K, R460 100K/F_4

R457	SP_715@499/F_4	TX2_HDMI+
R459	SP_715@499/F_4	TX2_HDMI-
R454	SP_715@499/F_4	TX1_HDMI+
R456	SP_715@499/F_4	TX1_HDMI-
R451	SP_715@499/F_4	TX0_HDMI+
R453	SP_715@499/F_4	TX0_HDMI-
R448	SP_715@499/F_4	TXC_HDMI+
R450	SP_715@499/F_4	TXC_HDMI-

UMA RS880M
715 ohm CS17152FB17

DIS Park-M2
499 ohm CS14992FB24

Close to HDMI Connector

EMI reserve for HDMI(HDM)

Close connector

TX2_HDMI+	R458 *100/F_4	TX2_HDMI-
TX1_HDMI+	R455 *100/F_4	TX1_HDMI-
TX0_HDMI+	R452 *100/F_4	TX0_HDMI-
TXC_HDMI+	R449 *100/F_4	TXC_HDMI-

HDMI HPD SENSE

UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin

[17] EXT_HDMI_HPD — R444 SW@10K_4 — +3V_D — Q33 SW@2N7002K

+3V — R187 10K/F_4 — Q16 2N7002K — HDMI_DET_R — R177 200K/F_4 — HDMI_DET — R176 200K/F_4

[9] INT_HDMI_HPD — +3V — R186 10K_4 — Q15 2N7002K — HDMI_HPD_EC# [34]

Close to HDMI Connector

[9] HDMI_DDC_DATA
[9] HDMI_DDC_CLK
RP20 *IV@0_4P2R_4 — HDMI_SDATA, HDMI_SCLK

UMA

DIS

[17] EV_HDMI_DDCCK — +3V — R443 SW@4.7K_4 — +5V — Q41 SW@2N7002K — HDMI_SCLK — R445 *SW@0_4

[17] EV_HDMI_DDCDAT — +3V — R614 SW@4.7K_4 — +5V — Q42 SW@2N7002K — HDMI_SDATA — R534 *SW@0_4

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HDMI PORT

CN17 SP@HDMI

TX2_HDMI+	1	D2+
	2	D2 Shield
TX2_HDMI-	3	D2-
TX1_HDMI+	4	D1+
	5	D1 Shield
TX1_HDMI-	6	D1-
TX0_HDMI+	7	D0+
	8	D0 Shield
TX0_HDMI-	9	D0-
TXC_HDMI+	10	CK+
	11	CK Shield
TXC_HDMI-	12	CK-
	13	CE Remote
HDMI_SCLK	14	NC
HDMI_SDATA	15	DDC CLK
	16	DDC DATA
	17	GND
HDMI	18	+5V
	19	HP DET
	20	SHELL1
	21	SHELL2
	23	GND
	22	GND

B2-TEST: +5V — F2 SMD1206P100TF — D6 RSX101M-30 — +5V_HDMI — HDMI_DET — C363 0.22u/6.3V_4

+5V — D21 CH501H-40PT — R446 2K/F_4 — HDMI_SCLK

+5V — D22 CH501H-40PT — R447 2K/F_4 — HDMI_SDATA

P/N: AOP---->DFHD19MR083
LTS---->DFHD19MR085

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Quanta Computer Inc.

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	HDMI	1A

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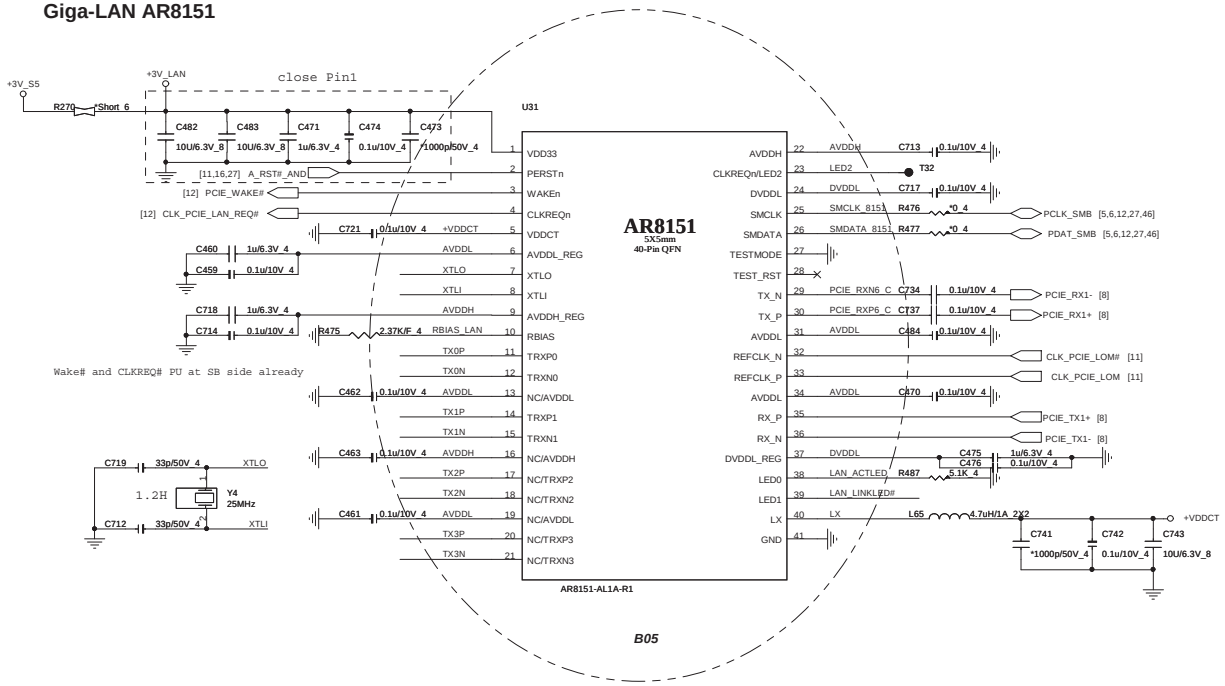
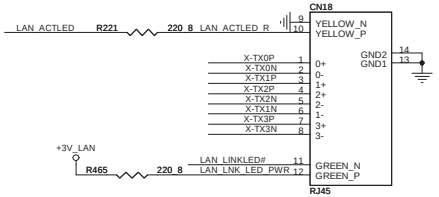
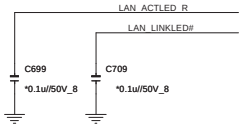
Giga-LAN AR8151

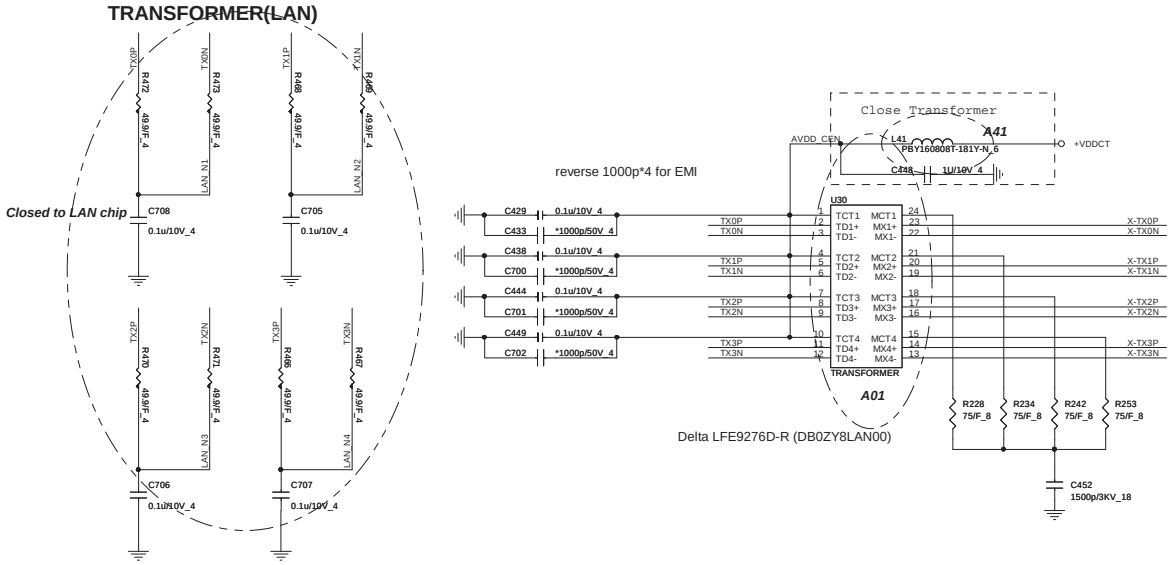


RJ45(LAN)





TRANSFORMER(LAN)



PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	LAN (AR8151)	1A

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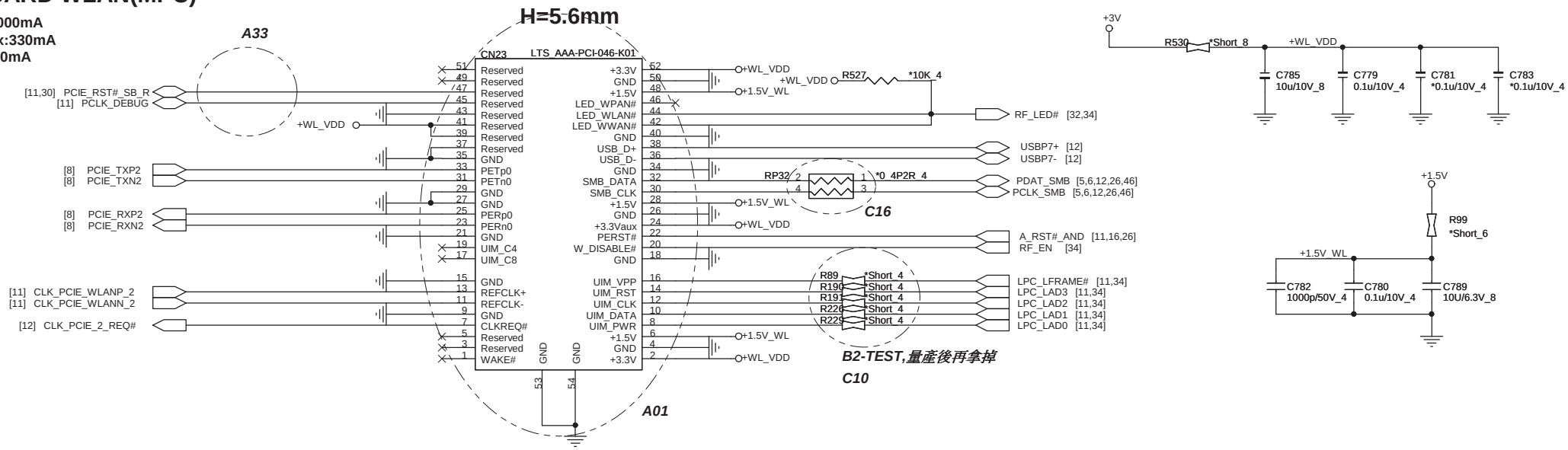
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1A
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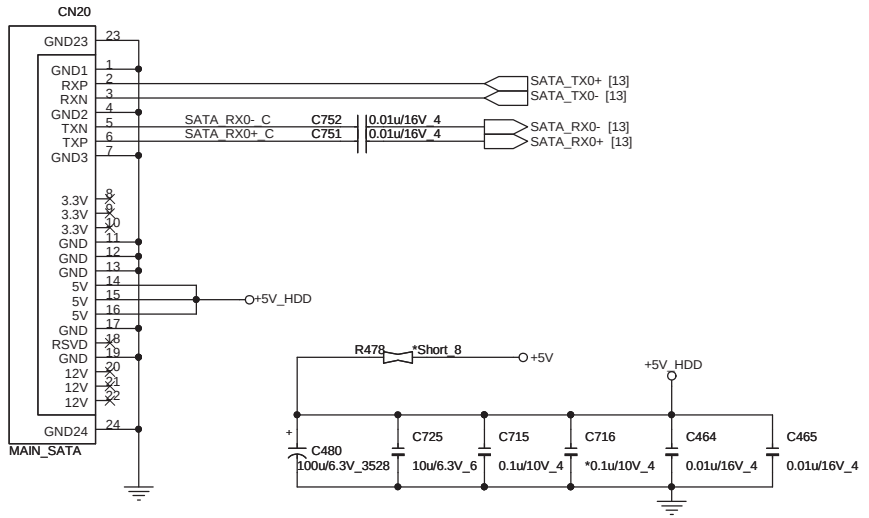
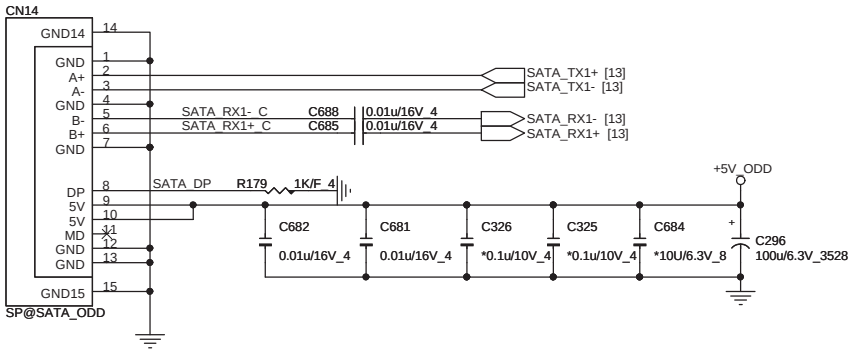
SATA HDD(HDD)



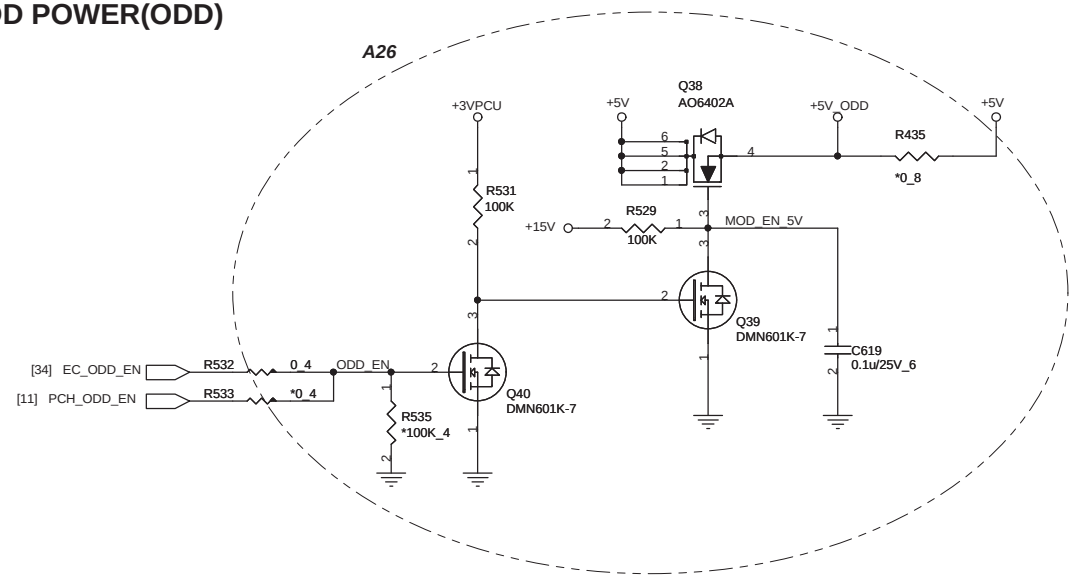
HOLE(OTH)

SATA ODD (ODD)



JM51(2-DIMM)-->CN14 P/N:DFHS13FR075
JV51(3-DIMM)-->CN14 P/N:DFHS13FR017
DFHS13FR022
DFHS13FR005
DFHS13FR006

ODD POWER(ODD)



PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD/ODD	1A
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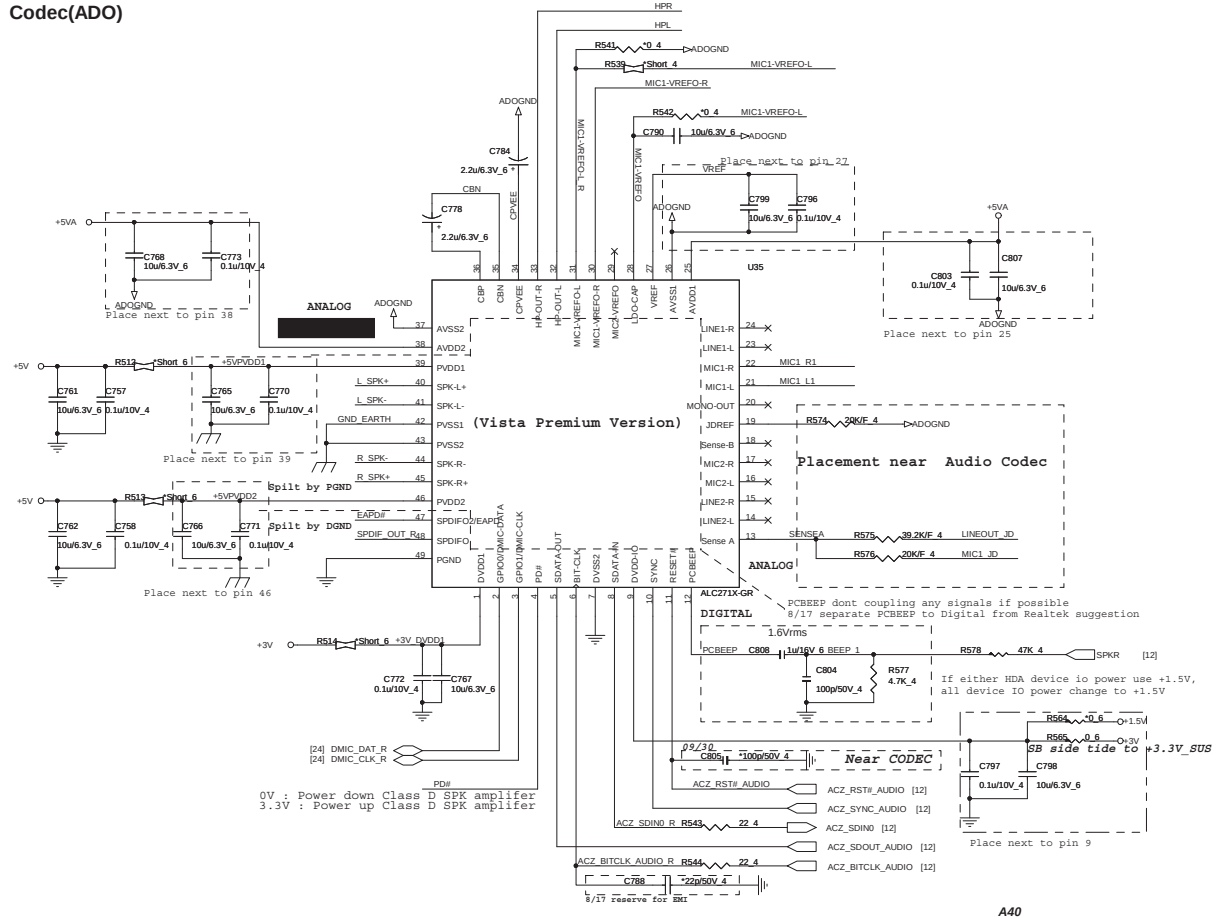
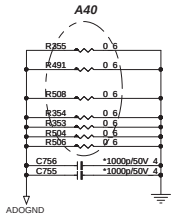
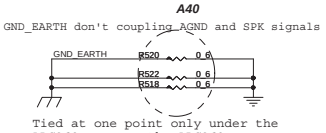
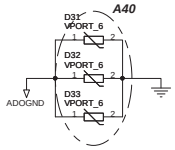
Codec(ADO)

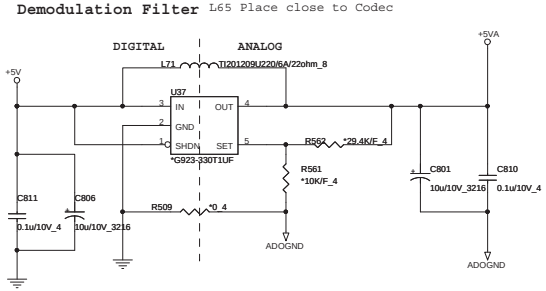








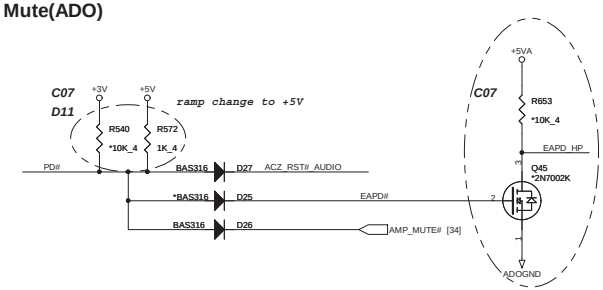
Power (ADO)



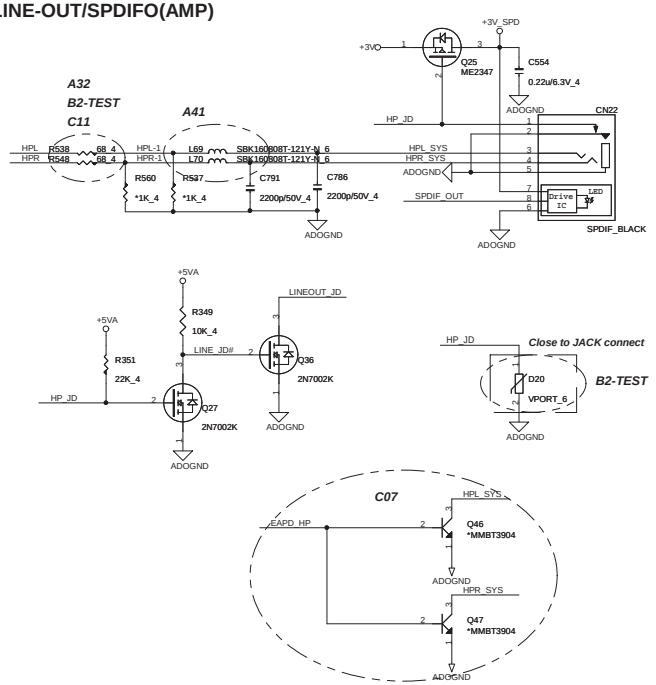
Vset =1.25V

Vout =Vset[1+AR(1,2)/AR(2,GND)]

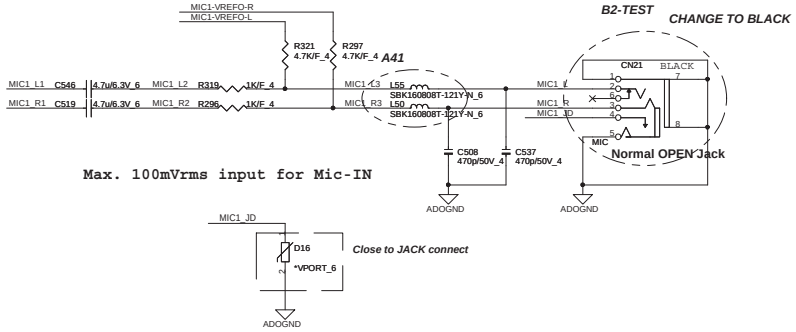
Mute(ADO)



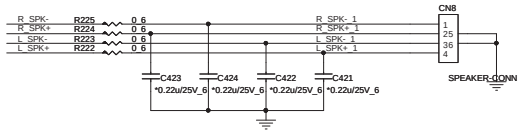
LINE-OUT/SPDIFO(AMP)



MIC(AMP)



Internal Speaker(AMP)



PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	ALC271X / AMP / SPK	1A

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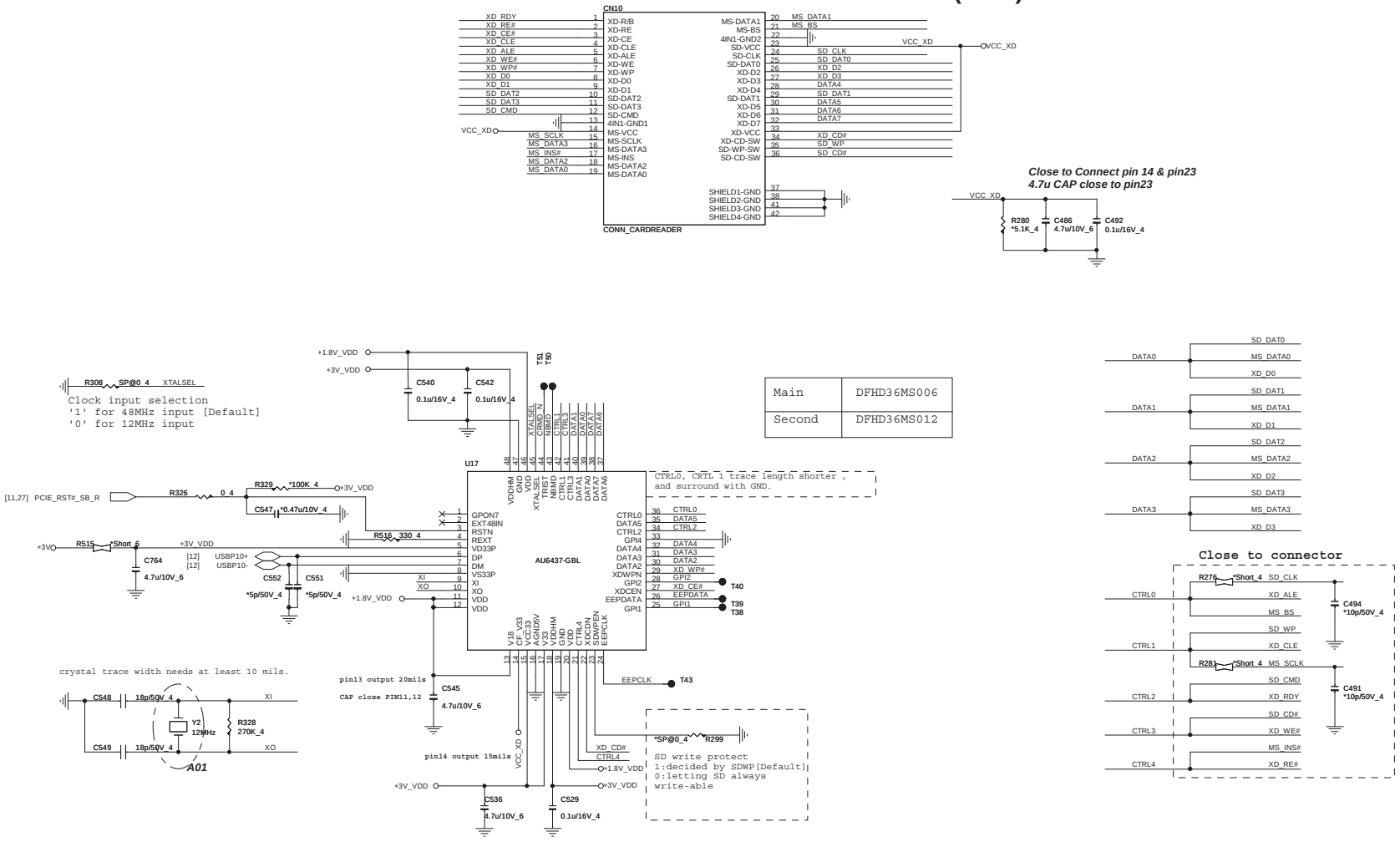
4 IN 1 CARD READER (MMC)



Main	DFHD36MS006
Second	DFHD36MS012

PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	AU6437 CardReader	1A

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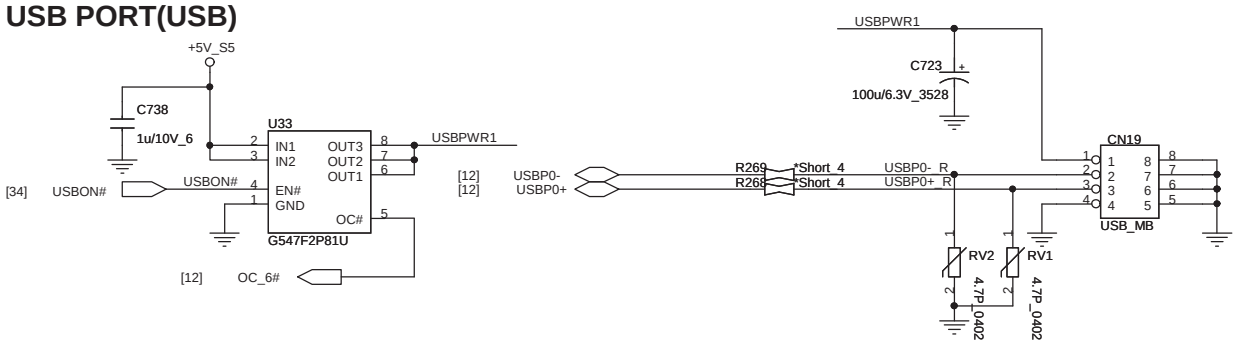
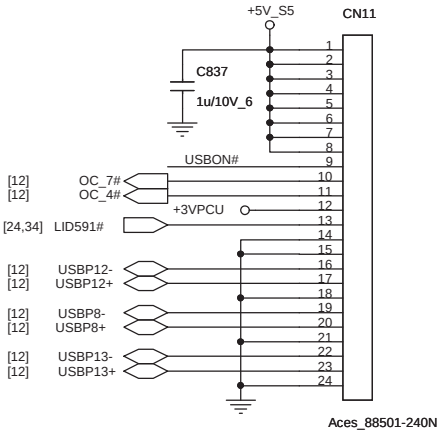
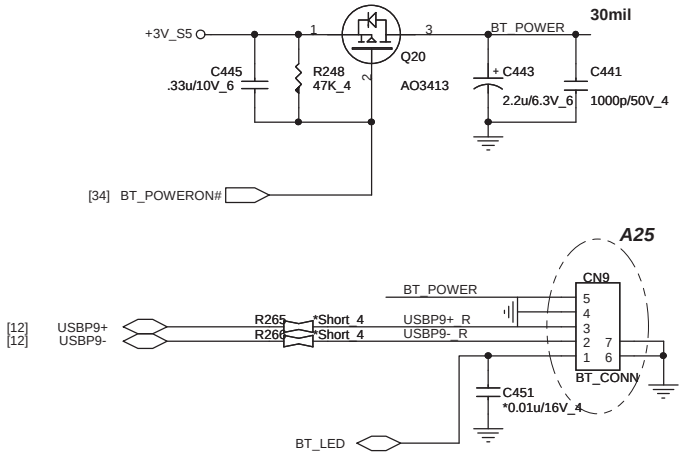
USB PORT(USB)



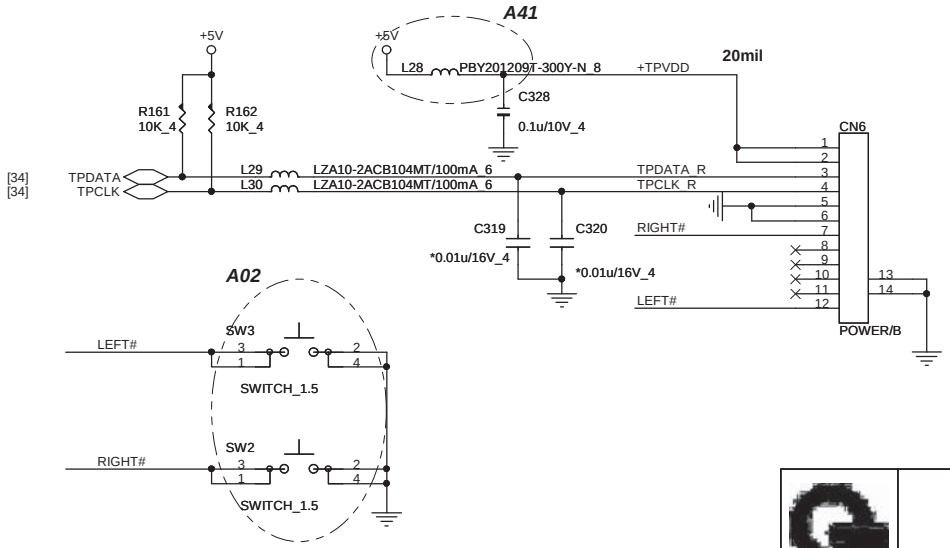
USB BOARD CONN(USB)



BLUETOOTH CONN(BTM)



TOUCHPAD BOARD CONN(TPD)



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Quanta Computer Inc.

Size	Document Number	Rev
	eSATA/USB	1A
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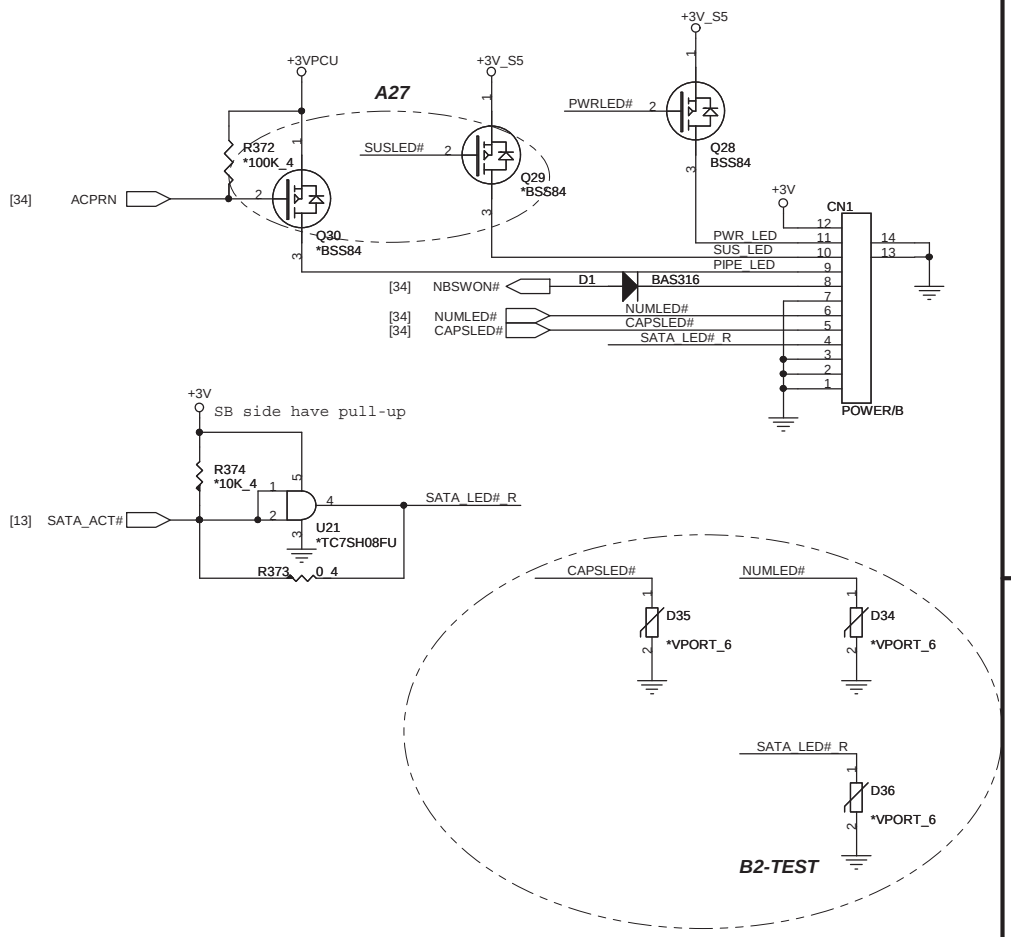
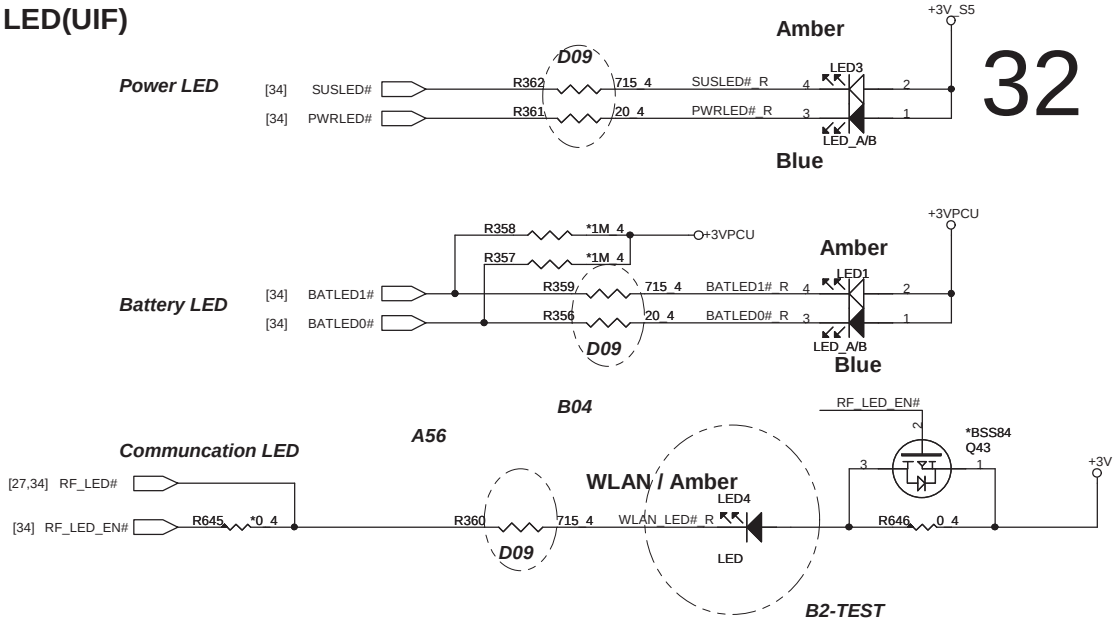
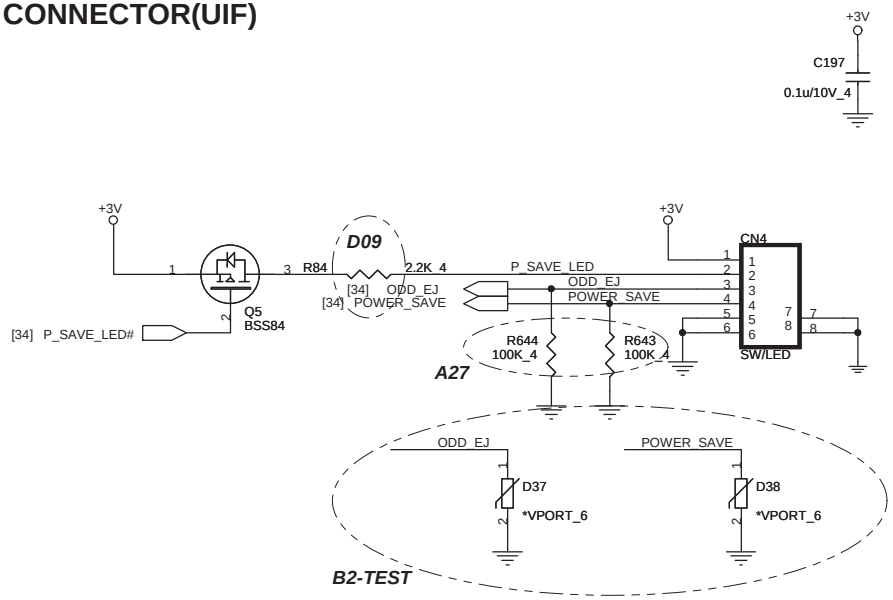
POWER BOARD CONN(UIF)



LED(UIF)



LED BOARD CONNECTOR(UIF)



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Quanta Computer Inc.

Size	Document Number	Rev
	POWER/USB/BT/TP/MDC	1A
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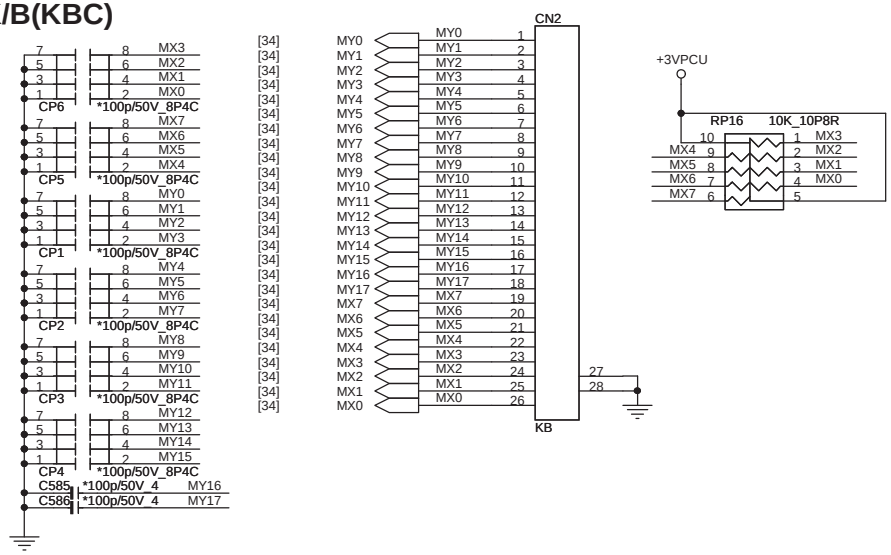
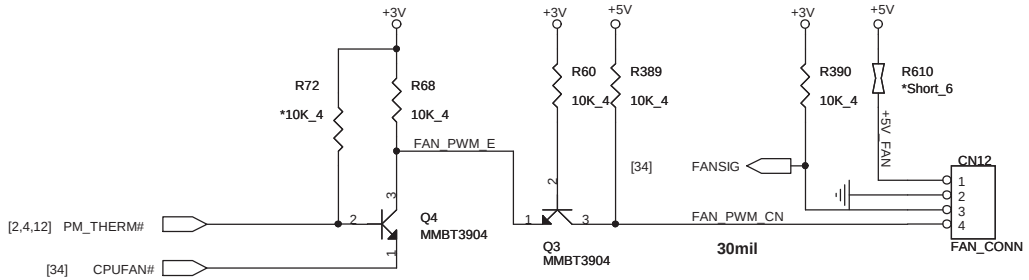
K/B(KBC)



CPU FAN(THM)



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Quanta Computer Inc.

Size	Document Number	Rev
	KB/FAN/EE RETURN CAP	1A

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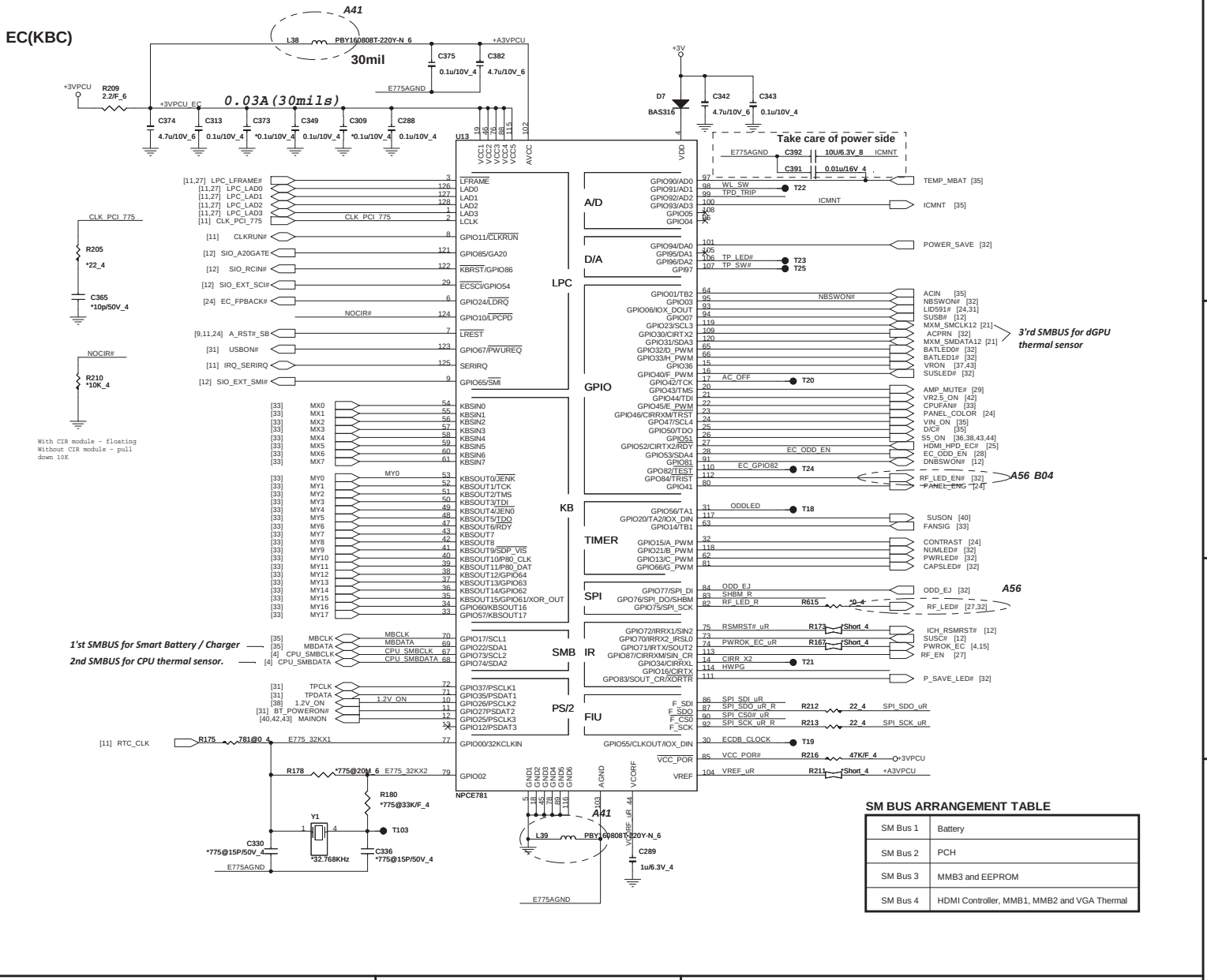
EC(KBC)

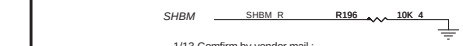


SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Thermal

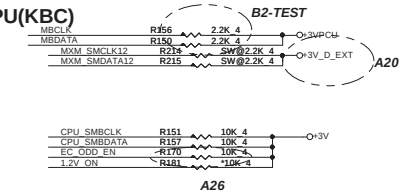
I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS



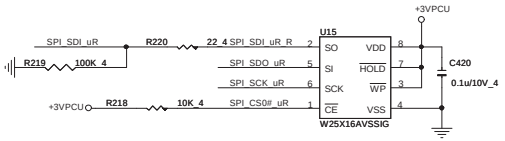
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)



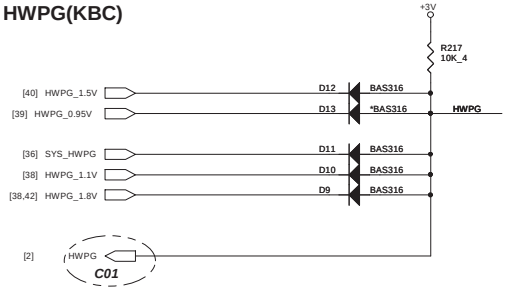
SPI FLASH(KBC)

U15 Change to 1M ==>AKE3GFK0Z09 / AKE3GZN0N00 / AKE3GZP0801

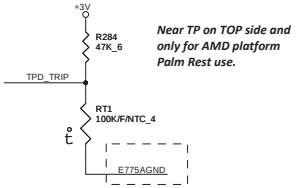


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

HWPG(KBC)

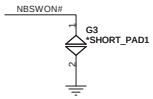


Palm Rest Thermal Sensor(THM)

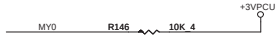


Near TP on TOP side and only for AMD platform Palm Rest use.

POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)



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Quanta Computer Inc.

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A

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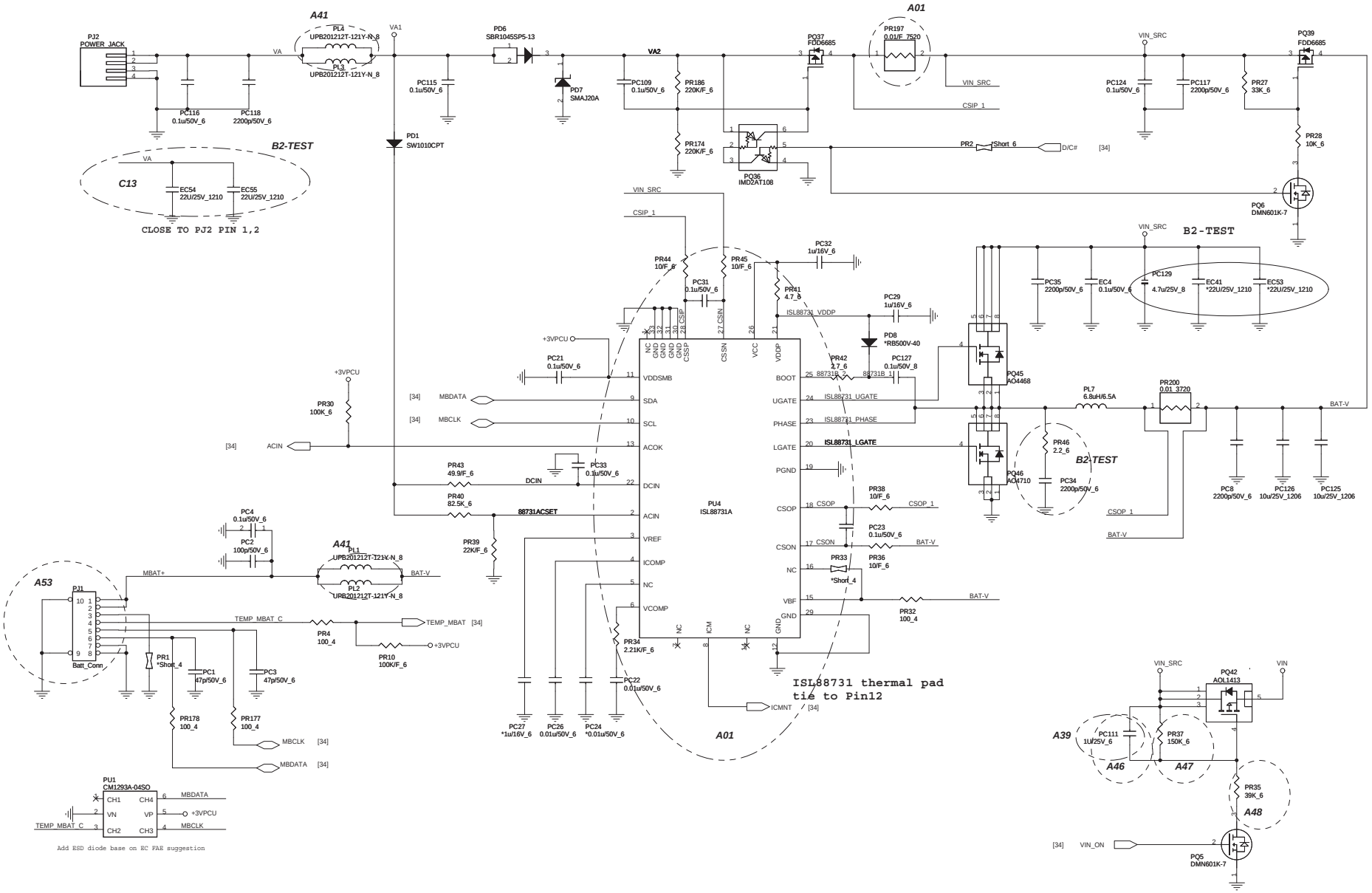
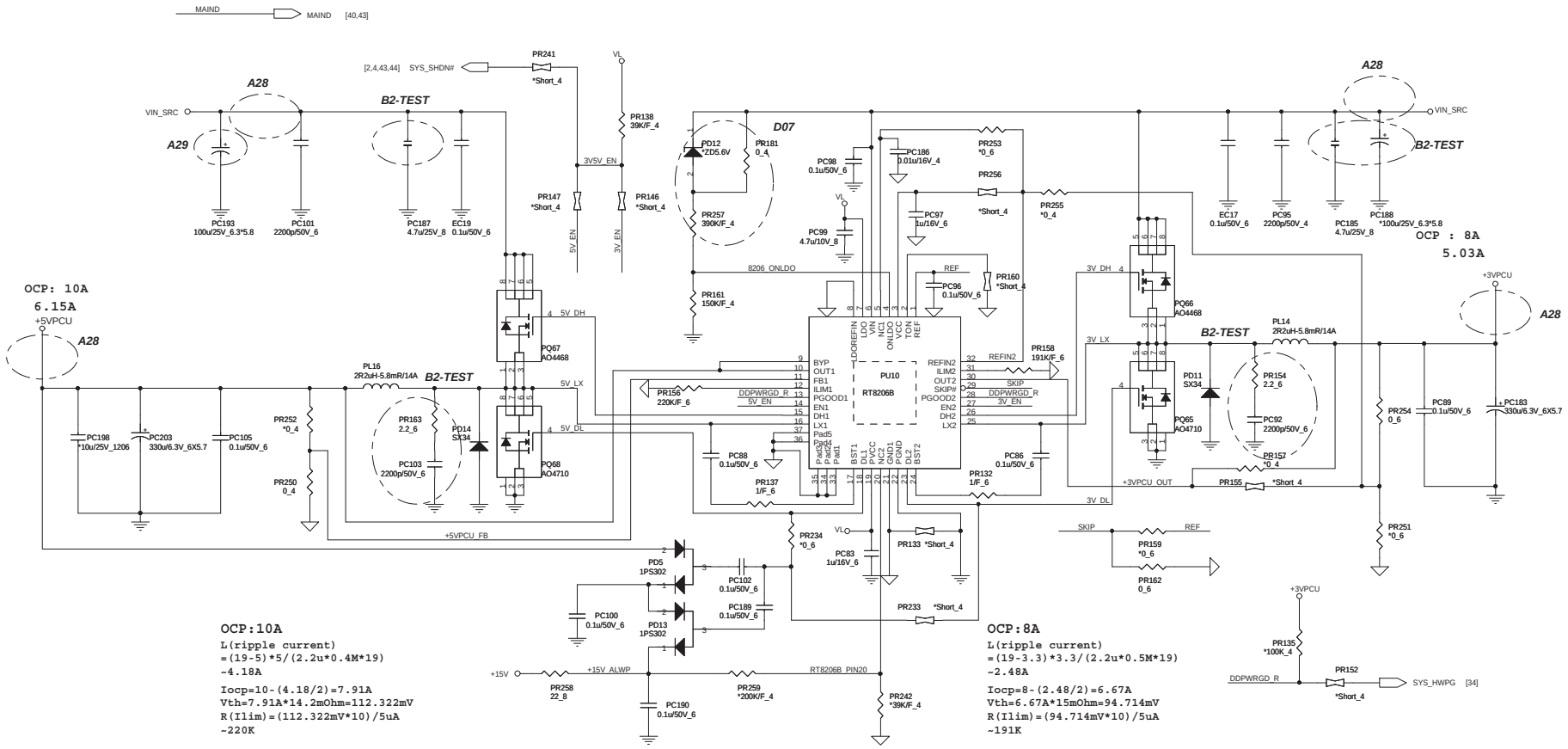


PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	CHARGER (ISL88731)	1A
Date: Wednesday, May 27, 2009	Sheet 35 of 49	



PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	SYSTEM 5V/3V (RT8206)	1A
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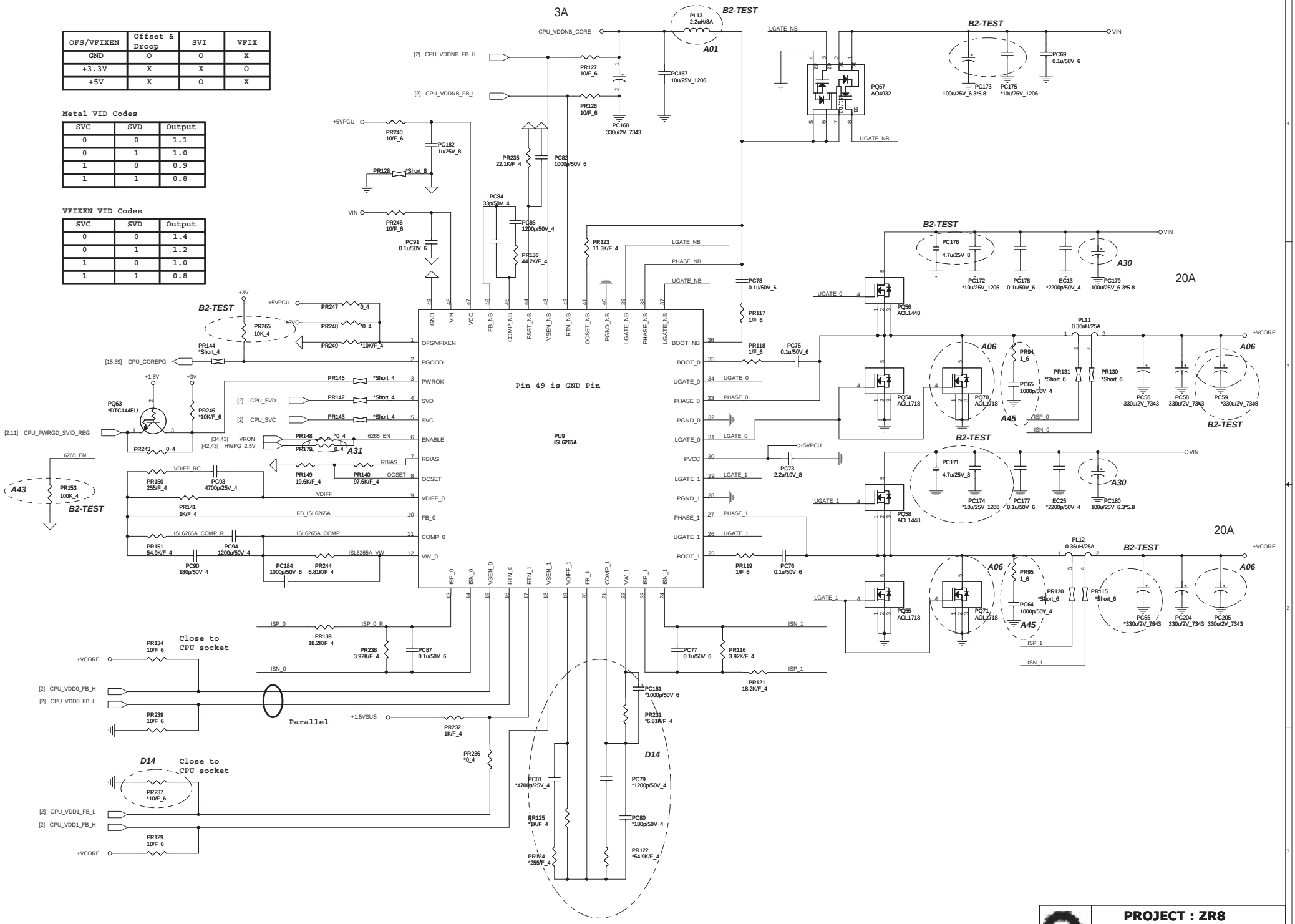
OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

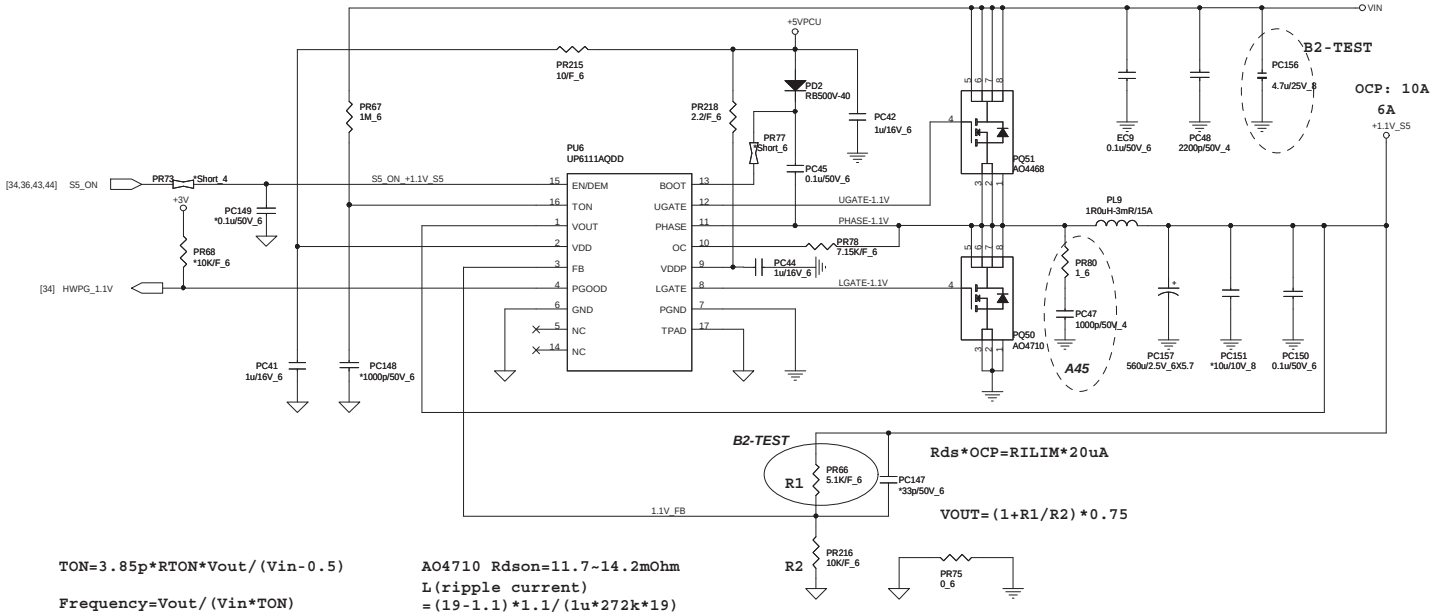
Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8





TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

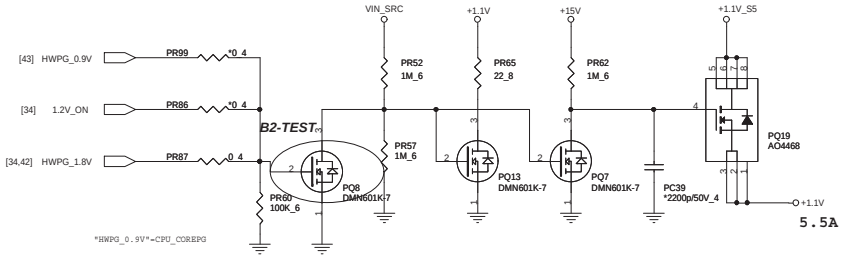
Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
~3.81A

14.2m*10=RILIM*20uA

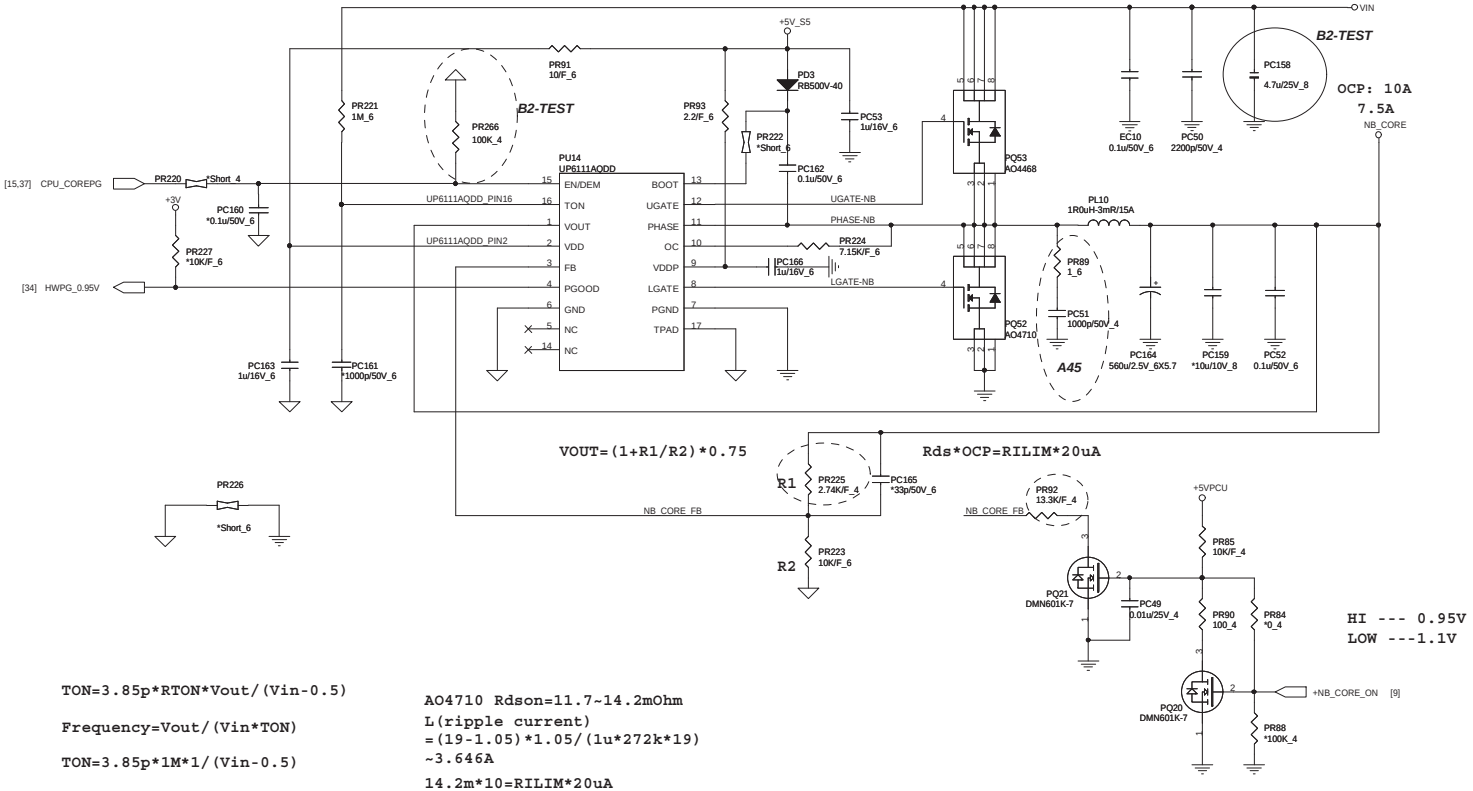
RILIM=7.1K--- 7.15K



PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	VCCP 1.1V(UP6111A)	1A
Date: Wednesday, May 27, 2009	Sheet 38 of 49	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

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Quanta Computer Inc.

Size	Document Number	Rev
	NB_CORE(UP6111A)	1A
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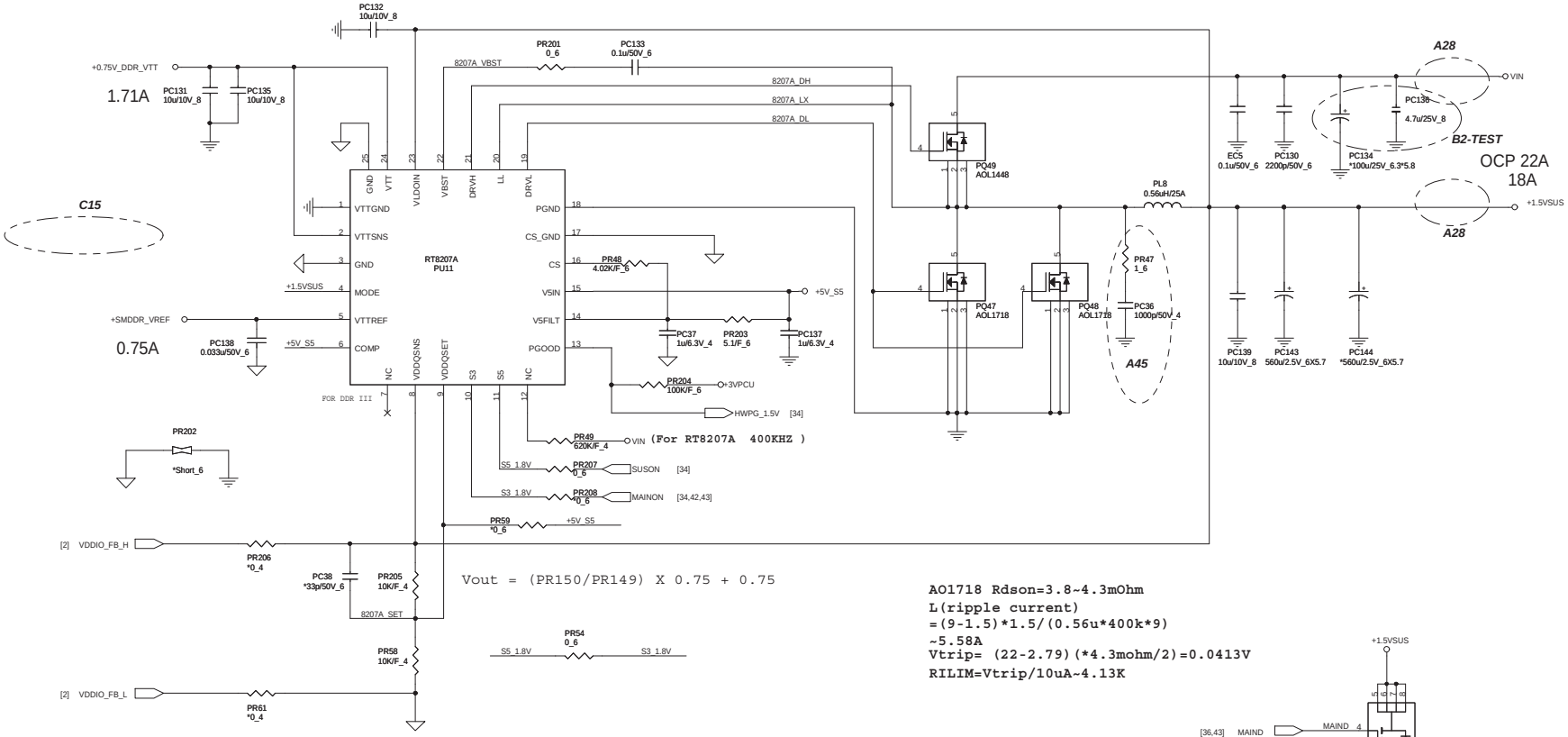
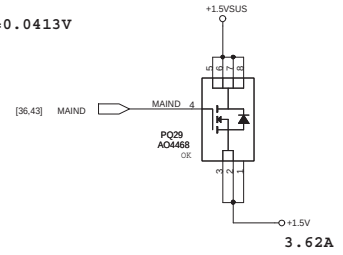
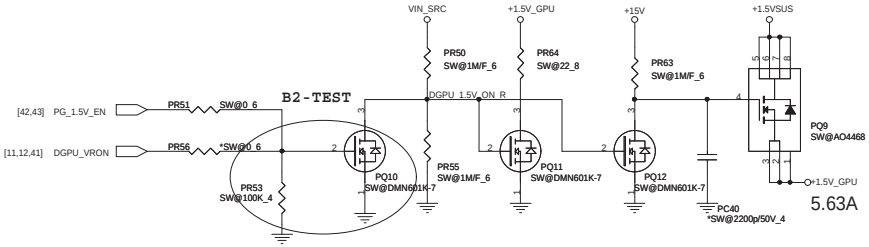
[PWM]



AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(9-1.5)*1.5/(0.56u*400k*9)
~5.58A
Vtrip= (22-2.79)(*4.3mohm/2)=0.0413V
RILIM=Vtrip/10uA~4.13K





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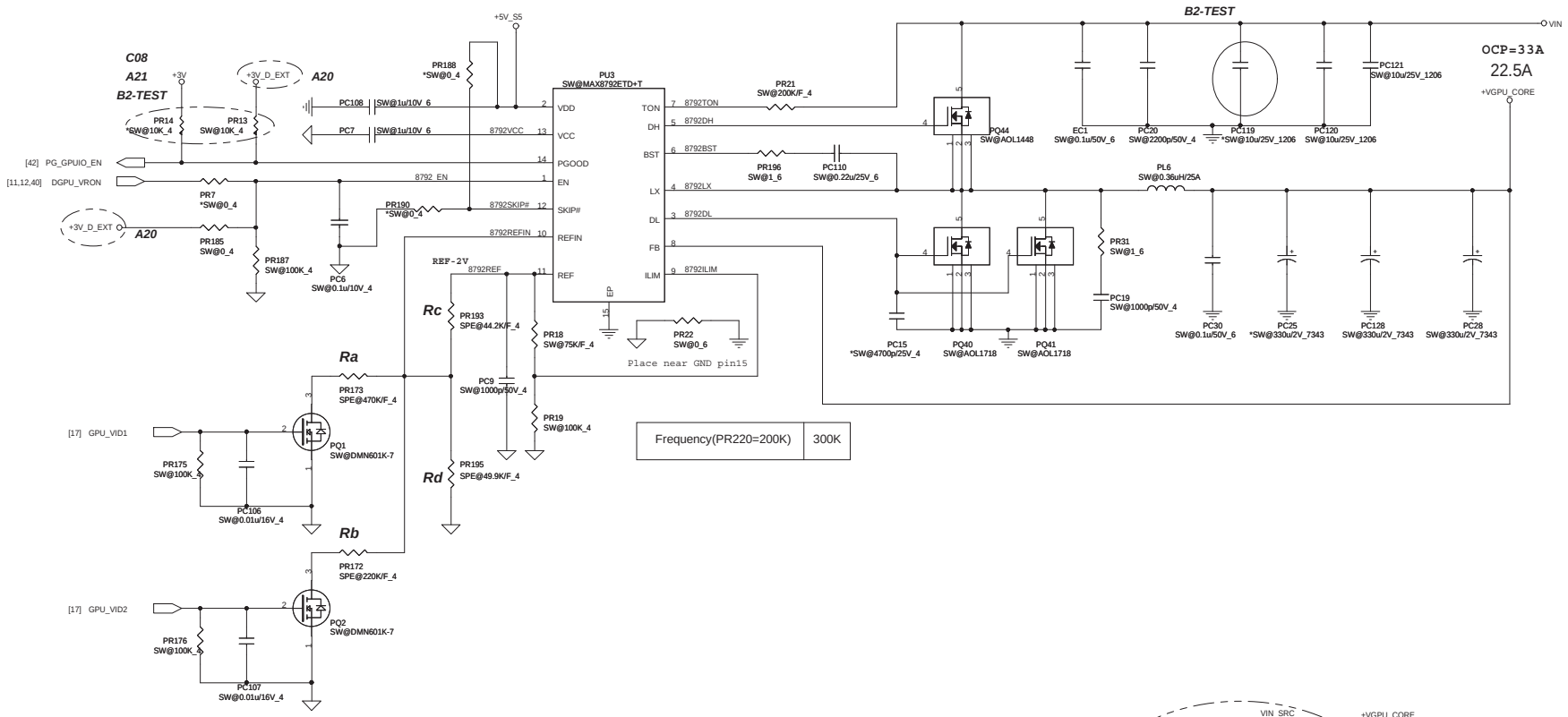
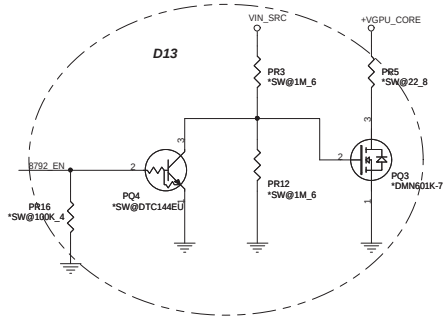
Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A
Date: Wednesday, May 27, 2009	Sheet 40 of 49	



Frequency(PR220=200K)	300K



Madison -Pro

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
1	1	0.9V

Ra	Rb	Rc	Rd	VREF
470K	220K	44.2K	49.9K	2V

Park -XT

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

Ra	Rb	Rc	Rd	VREF
332K	130K	39.2K	49.9K	2V

A03

Rc --> 39.2K/F_4 (CS33922FB15)
Ra --> 332K/F_4 (CS43322FB15)
Rb --> 130K/F_4 (CS41302FB00)

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Quanta Computer Inc.

Size	Document Number	Rev
	GPU CORE(MAX8792)	1A

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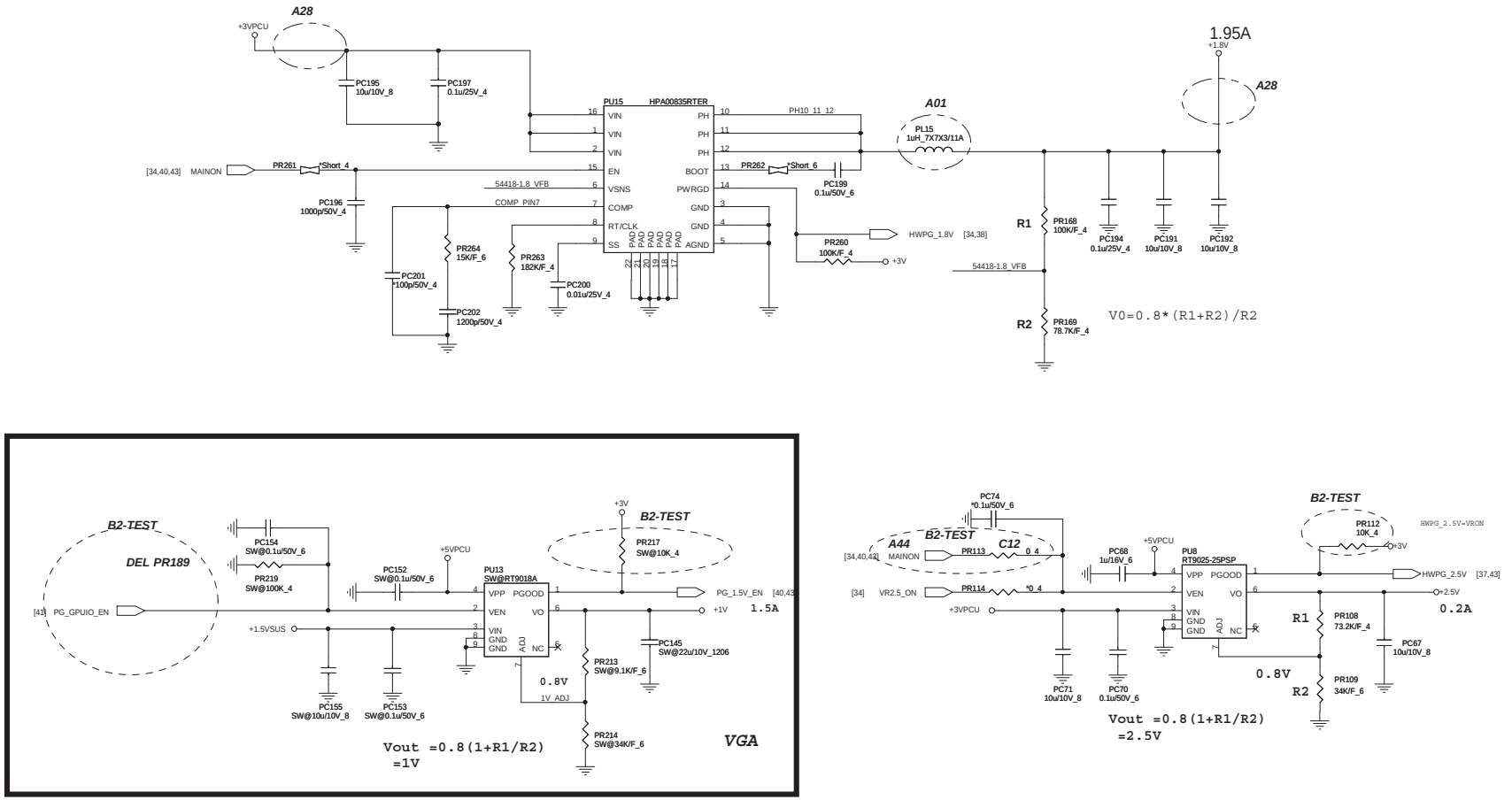

PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (2.5V/1.8V)	1A
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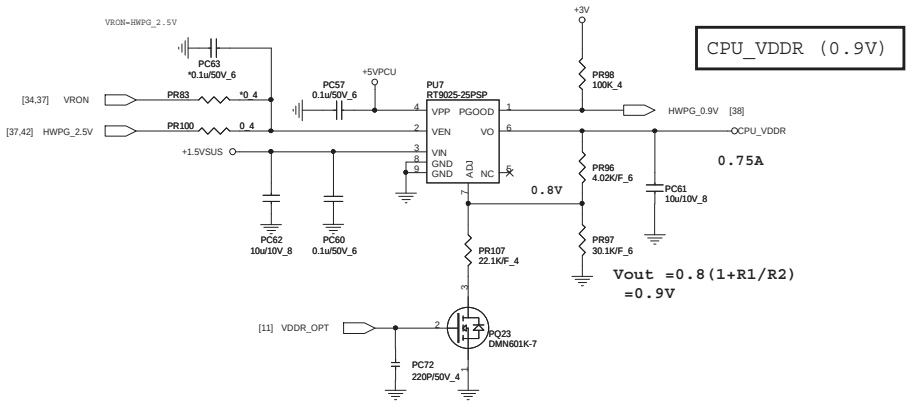
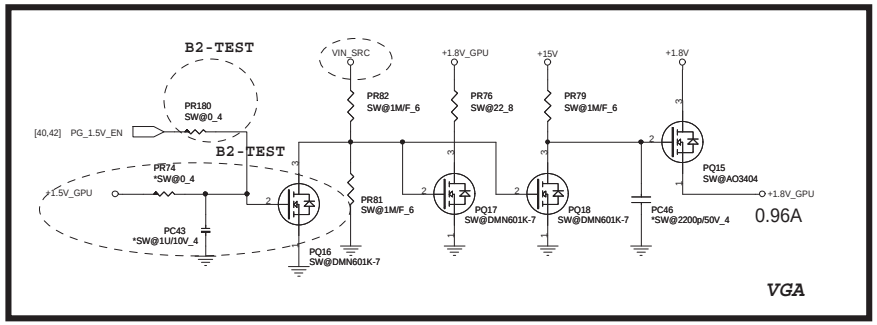
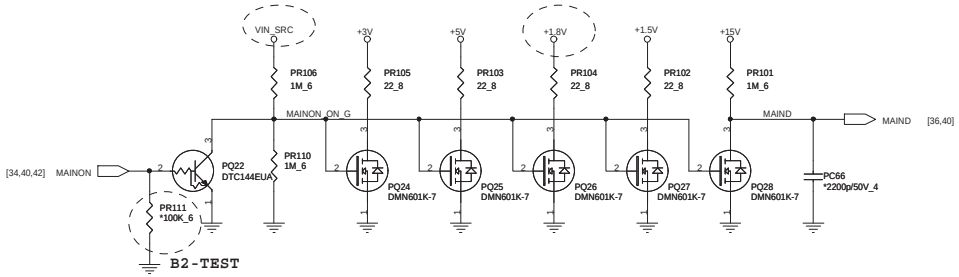
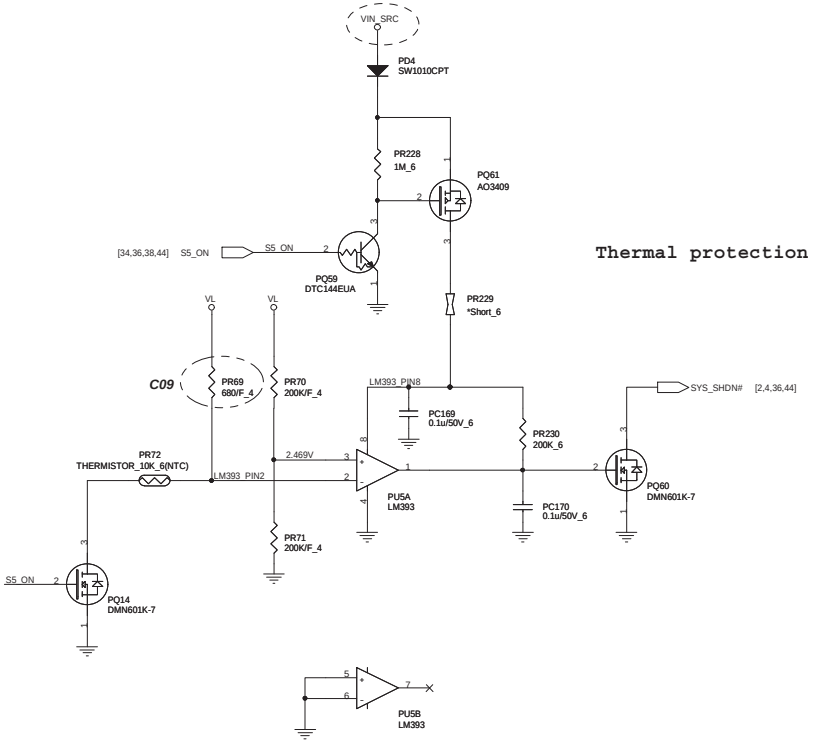






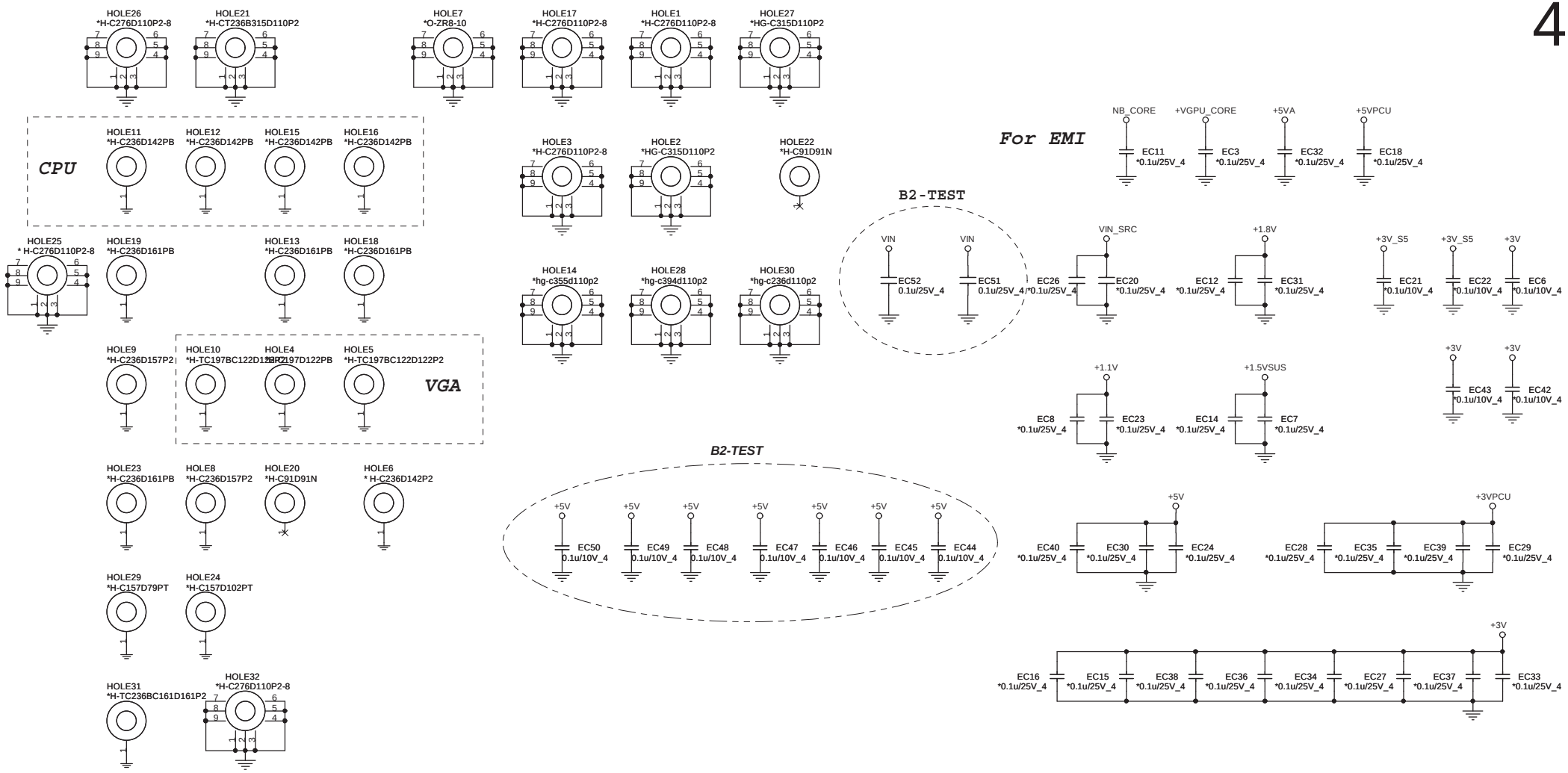


For EC control thermal protection (output 3.3V)

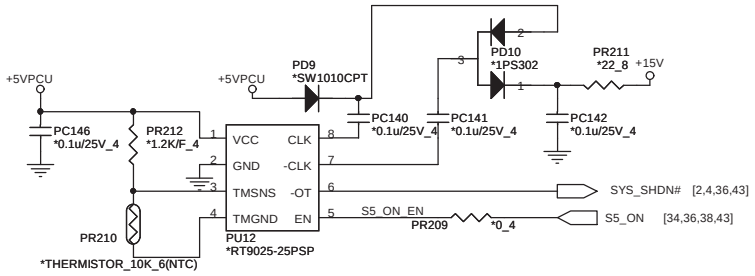
PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge /Thermal protection	1A
Date: Wednesday, May 27, 2009	Sheet 43 of 49	



POWER TEST

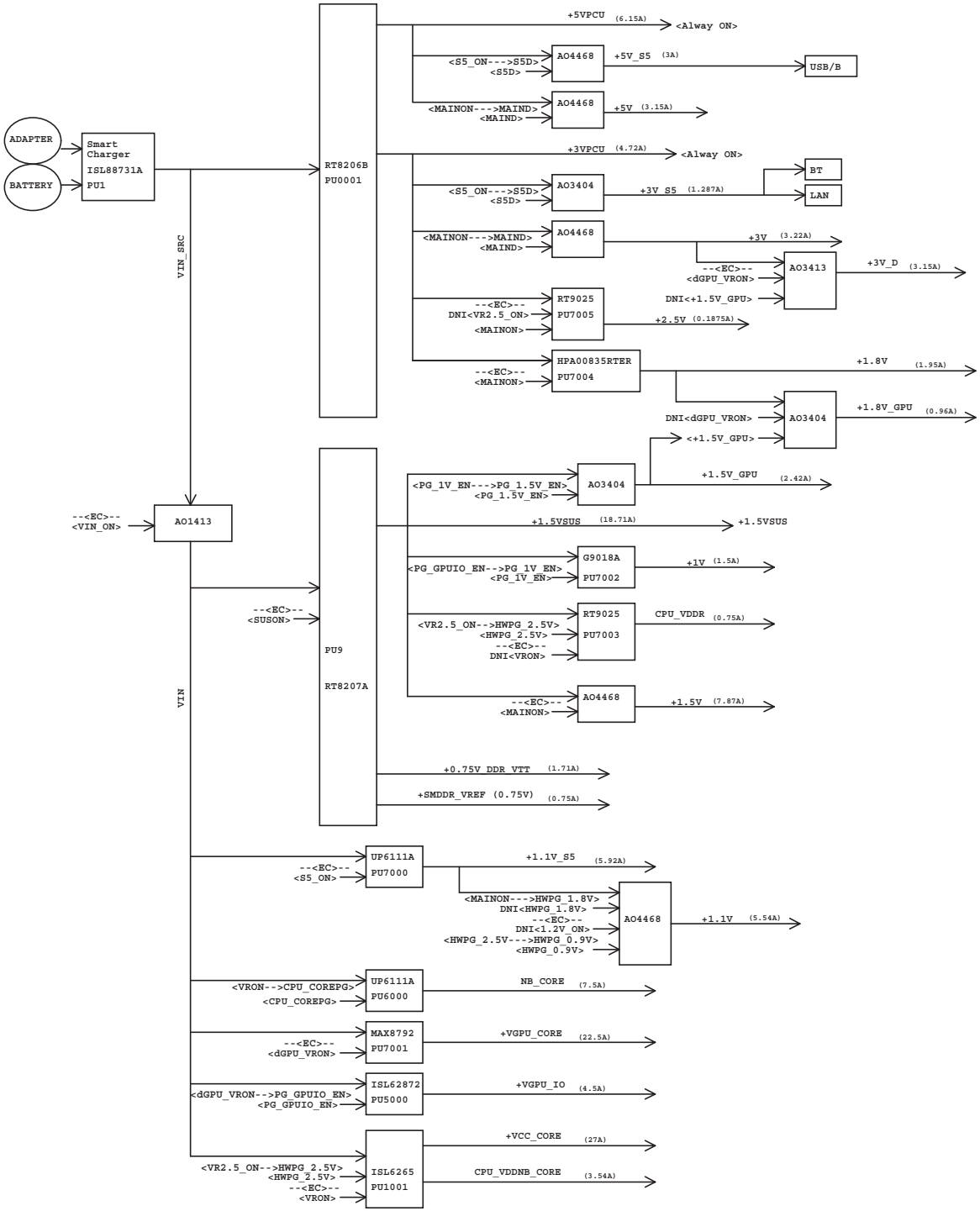


PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	Hole, Nuts	1A
Date: Wednesday, May 27, 2009	Sheet 44 of 49	

ZR8 Power tree



PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	Power Tree	1A

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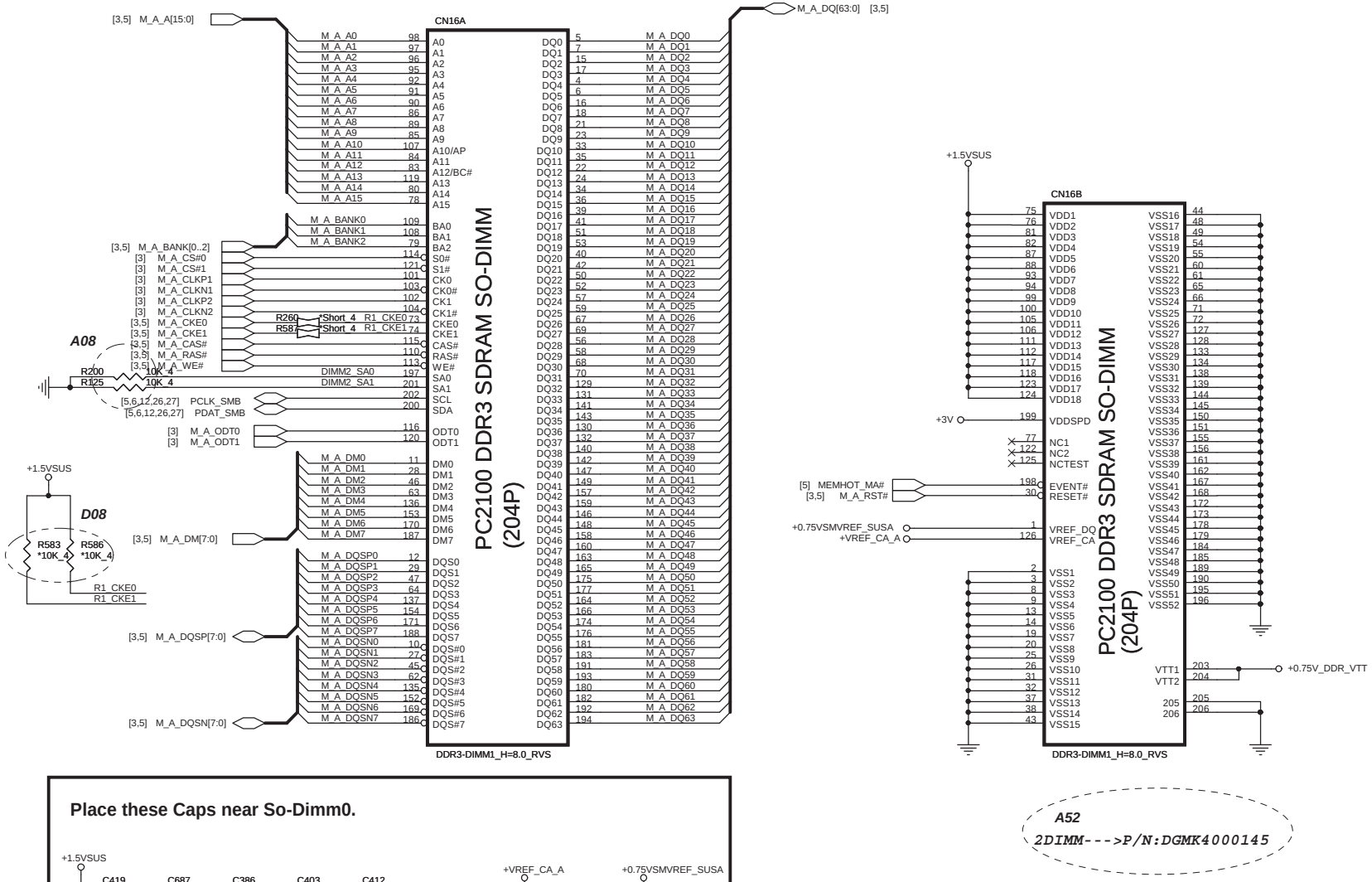
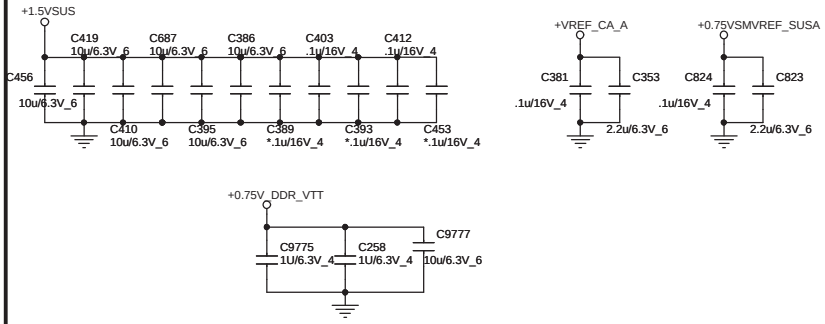
DDR3 (DDR)



Place these Caps near So-Dimm0.



PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 DIMM-1(H=9.2)	1A

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ZR8 Schematic EC Tracking Record A (For A TEST) Nov.17 , 2009
EC / Page / Item / Description

A01 Page25/27/28/31/32/36/38/44 Change footprint , due to SMT open issue highlight.
A02 Page32 Change T/P switch P/N, due to SMT open issue highlight.
A03 Page42 Modify Madison-Pro & Park-XT VID table.
A04 Page14 Modify board ID table and R517,R304 support Side-port function.
A05 Page14 Add R528 support different Side-port VRAM type.
A06 Page44 Support CPU 45W solution.
A07 Page02 Change clock gen to no stuff, due to use internal clock source.
A08 Page06/07/48 Change SO-DIMM SMBUS address.
A09 Page08/10/11 Add Side-port function.
A10 Page10 Chane HDMI DDC CLK/DATA port.
A11 Page10 Stuff R190.
A12 Page12 Change dGPU_PWROK from GPIO1 to GPIO32.
A13 Page12 Change board ID GPIO pin.
A14 Page13 1. Stuff D19,R307,C538 and no stuff D18. 2. Change pull high power rail from +3V_D to +3V.
A15 Page16 Change R500 from 0ohm to 10k.
A16 Page12 Connect 25Mhz for GPU workaround design.
A17 Page18 Modify GPU Power-on sequence table.
A18 Page18 Remove GPU_IO VID contron pin and change GPU_CORE GPIO pin to GPIO15/20.
A19 Page19 Change R107 from 680ohm to 51 ohm and modify design of MEM_RST#. Also change R30 to no stuff.
A20 Page20/22/35/42 Reserve +3V_D_ZR8 power rail for GPU leakage issue.
A21 Page18 Reserve VGA_REQ# pin.
A22 Page25 Delete brightness switch IC control and change to 0ohm solution.
A23 Page25 Stuff R135,R144 ,due to some CRT monitor can't display.
A24 Page25 Stuff C776,C787 for EMI request.
A25 Page25/32 Change connect footprint and P/N.
A26 Page29/35 Add ODD power switch design and stuff R170.
A27 Page33 Change Q29,Q30 to no stuff.
A28 Page37/41/44 Remove jmuper.
A29 Page37 Change PC193 P/N to low highlimit, due to ME thermal door impact.
A30 Page38 Change PC179,PC180 from 22uF/25V to 100uF/25V.
A31 Page38 Change CPU_CORE enable from VRON to HWPG_2.5V.
A32 Page30 Change R538,R548 from 48ohm to 68ohm for audio performance.
A33 Page28 Change R572,R563 to short pad for debug use.
A34 Page20 Change +VGPU_IO power rail to +VGPU_CORE.
A35 Page25 Connect CN5 LCD connect shielding pin to GND for ESD issue.
A36 Page18 Change R65 to no stuff.
A37 Page22 Reserve OVERT# pull high resistor prevent noise.
A38 Page33 Add pull low 100k ohm for ODD_EJ,POWER_SAVE signal.
A39 Page36 Reserve cap for power team request.
A40 Page30 Stuff 0 ohm resistor for ESD protect use.
A41 Page02/03/10/11/15/18/20/21/27/30/32/35/36 Change bead P/N for EMI request, the reason is cost down and not STD parts.
A42 Page21 Reserve 0 ohm for PLL power use.
A43 Page38 Remove PR153 & change to 0402 package
A44 Page44 Change PR113 from 0 to 10K Ohm & Change enable source to +3V
A45 Page38/39/40/41 Stuff PR80,PR89,PR94,PR95,PR47 to 1 Ohm & PC47,PC51,PC64,PC65,PC36 of value to 1000p for EMI request
A46 Page36 Change PC111 of value to 1U/25V
A47 Page36 Change PR37 of value, from 33K to 150K
A48 Page36 Change PR35 of value, from 10K to 39K
A49 Page26 Change HDMI connector PN
A50 Page7 Change P/N for 3-DIMM H=4.0 STD
A51 Page6 Change P/N for 3-DIMM H=4.0 RVS
A52 Page48 Change P/N for 3-DIMM H=8.0 RVS
A53 Page36 Change battery connector P/N to DFHD08MR099
A54 Page26 Modify HDMI's I2C for DIS.

ZR8 Schematic EC Tracking Record A (For A TEST) Nov.17 , 2009
EC / Page / Item / Description

A55 Page14 Change board ID power rail from +3V_S5 to +3V.
A56 Page33/35 Modify WLAN RF_LED control design.
A57
A58 Page12 Remove R331 only for A11 version.
A59 Page12 Add U18,C533 & remove R303 for power sequence.
A60 Page14 Remove C760,C754,R507& Y7, due to it's for external clock use.
A61 Page2 Stuff R474,R486 for LAN & WLAN of REQ#.
A62 Page3/12 Stuff R424 and no stuff R286, due to CPU_PRPCHOT# is +1.5VSUS level.
A63 Page16 Change D29 package & Add D24.

Note : Change 0ohm to short pad
R276,R281,R415,R443,R445,R531,R532,R533,R534,R535,R539,R566,R174,R512,R513,R263,R437,R439,R441,R99

ZR8 Schematic EC Tracking Record B1 (For B1 TEST) Dec.09 , 2009
EC / Page / Item / Description

B01 Page21 Remove DP/TMDS Output Driver Analog Supply from port C&D. Due to it's don't to use.
B02 Page25 Stuff R48 for Discrete platform use.
B03 Page/10/25 Modify R signal pull low resistor value to 140ohm, due to keep 70 ohm trace impedance.
B04 Page33 Modify WLAN LED design and change from GPIO82 to GPIO84.
B05 Page27 Change LAN layout footprint for "SAW" new package.
B06 Page13/25 Reserve CCD USB host from for Port2, due to CCD issue.
B07 Page33 Reserve blue LED power source to 5V, due to White/Blue LED max Vf is more than Green/Orange LED.

ZR8 Schematic EC Tracking Record C (For C TEST) Jan.28 , 2010
EC / Page / Item / Description

C01 Page02/34 Remove "CPU_THERMTRIP#" control from SB820, due to BIOS don't support this function. Add another "SYS_SHDN#" for H/W shutdown function and add HWPG shutdown design.
C02 Page04 No stuff Q21,D14,R255 for thermal sensor Alert fnction and change to EC or H/W shutdown function.
C03 Page09 Add 1uF for monitor test noise issue.
C04 Page12 Add 0ohm to separate VGA_REQ function, due to it's don't support the function and cause by leakage current concern.
C05 Page24 Modify VGA note text for R signal impedance control.
C06 Page24 Add brightness switch control by iGPU switch mode. Due to BIOS for C test already support.
C07 Page29 Reserve EAPD# audio design for "Bo" sound.
C08 Page41 Change PG_GPUIO_EN pull high power rail from +3V to +3V_D_EXT. For Park GPU SG mode hang up issue.
C09 Page43 Change PR69 FROM 1.2K to 680ohm , the reason is for SDA high temperature (40 degree/20% humidity) auto shutdown issue.
C10 Page27 Short LPC signal for debug card use.
C11 Page29 Change R538,R548 from 56ohm to 68ohm for audio performance test FSOV spec requirement.
C12 Page42 Change PR113 from 10k to 0ohm.
C13 Page35 Change EC54,EC55 to stuff for ISN issue.
C14 Page21 Modify DDR3 Memory Aperture size table.
C15 Page03/40 Reserve VDDR_SENSE signal to controller IC.
C16 Page27 Change RP32 to no stuff.
C17 Page04 Modify CPU thermal control design from EC or BIOS control and change U16,R254 to no stuff ,Q17,Q18,Q19 to stuff.
C18 Page03 No stuff R189.

Note : Change 0ohm to short pad
R124,R121,R174,L31,L37,L35,R136,R115,R169,R325,R315,R295,R292,R278,R31,R90,R21,R112,R24,R25,R270,R530,R99,R478,R512,R513,R514,R326,R269,R268,R265,R266,R610,PR73,PR220,PR261
,PR229

ZR8 Schematic EC Tracking Record A (For Ramp) Feb.25 , 2010
EC / Page / Item / Description

D01 Page03 Change CPU VDDR_SENSE pull high power rail to CPU_VDDR and remove trace connect to controller IC.
D02 Page15 Modify text note.
D03 Page12 Change "GBE_COL" ,"GBE_CRS" ,"GBE_RXERR" to GND follow SCL V1.04 version.
D04 Page14 Change USB PLL power rail source to separate VDDPL_33_USB_S follow SCL V1.04 version.
D05 Page04 No stuff R267,C450,C344.
D06 Page09 Delete R149,R152 layout pad.
D07 Page36 No stuff PD12 and add PR181, change PR257 from 1k to 390k. The purpose is for panasonic battery low power protect issue.
D08 Page05/46 No stuff R584,R259,R583,R586 for CKE signal.
D09 Page32 Change LED current sense resistor value for LED light measure requirement. (Follow ZR7B)
D10 Page21 Modify VRAM table.
D11 Page05/06 Change R123,R122,Q10,R202,R195,Q14 to no stuff, due to S1g4 don't support MEMHOT function.
D12 Page02 Reserve prochot# for FAN control.
D13 Page41 No stuff PR16,PQ4,PR3,PR12,PR5,PQ3. Due to MAX8792 had integrate discharge design.
D14 Page37 Change some component to no stuff, dut to for S1g4 use the same VDD power don't need to compensation difference voltage.

Note : Change 0ohm to hort pad.
R203,117,R585,R588,R260,R587,PR1,PR2,PR33,PR241,PR147,PR146,PR160,PR256,PR133,PR233,PR152,PR155,PR128,PR142,PR143,PR144,PR145,PR130,PR131,PR115,PR120,PR77,PR226,PR222,PR202,PR262.